UNIVERSIDAD COMPLUTENSE DE MADRID
FACULTAD DE CIENCIAS FÍSICAS
DEPARTAMENTO DE FÍSICA DE MATERIALES

TESIS DOCTORAL

Fabrication of etching masks and electronic nanodevices by oxidation scanning probe lithography

MEMORIA PARA OPTAR AL GRADO DE DOCTOR

PRESENTADA POR

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Madrid, 2015

Universidad Complutense de Madrid
Facultad de Ciencias Físicas
Departamento de materiales

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Dissertation submitted by

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For the degree of doctor in philosophy

Supervised by Prof. Ricardo Garcia at Instituto de Ciencia de Materiales de Madrid, CSIC

Madrid, October 2014

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Facultad de Ciencias Físicas
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Fabricación de máscaras y nanodispositivos electrónicos mediante nanolitografía de microscopía de fuerzas

Tesis para optar al grado de Doctor en Ciencias Físicas
Presentada por

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Dirigida por el Prof. Ricardo Garcia en el Instituto de Ciencia de Materiales de Madrid, CSIC

Madrid, Octubre de 2014

Financiación

La presente tesis ha sido realizada en el grupo ForceTool en las siguientes instituciones:

- Instituto de Microelectrónica de Madrid, CSIC
- Instituto de Ciencia de Materiales de Madrid, CSIC

Financiada mediante una beca predoctoral del programa FPI del Ministerio de Ciencia e innovación, con referencia: BES-2010-035491 MAT2009-08650 y el proyecto europeo F7 'Single Nanometer Manufacturing beyond CMOS'

A Ok Hee.

Acknowledgements

Ricardo, me alegro de haber hecho la tesis en tu grupo y bajo tu dirección. La ciencia y la labor investigadora han resultado mucho más difíciles, frustrantes y diferentes de lo que pensaba antes de comenzar la tesis, pero siguen pareciéndome igual de interesantes y aún no he descartado la posibilidad de desarrollar una carrera científica.

He tenido suerte con los compañeros de grupo que me han tocado: Marta, Christian, Elena, Jorge, Marco, Amir, Horacio, Andra, Alma, Dani, Ana, Fran y Pablo. Gracias por hacer el lugar de trabajo un sitio cómodo y por todas las horas de diversión fuera del trabajo. En particular, gracias, Ana, por esforzarte siempre por hacerme la vida más fácil en las cosas burocráticas y por traer polémicas sobre cine, literatura y tíos macizos; gracias, Fran, que apareciste para compartir con alguien las penas de la oxidación local y gracias, Marco, por ser siempre generoso, paciente y una mente racional y madura con la que contar.

Me gustaría agradecer a Javier Martínez lo que me enseñó al principio de la tesis y luego, su disposición a escucharme y echar un cable cuando le he consultado. A Fernando por ayudarme con el programa de litografía. Gracias Marga por los consejos y las conversaciones ameno-didácticas.

Mil y una gracias al profesor Jose Luis Vicent por el interés y aprecio que ha mostrado por mí desde los años de carrera en el alma mater.

¿Qué supondría hacer una tesis sin tener amigos con los que quejarse amargamente o desconectar de ella? Chicos de 'Polonia', ¡qué despacho más acogedor construimos!, con cafetera incluida; Jara, ojalá coincidiéramos más; Iñaki, cómprate una mascota y deja de asustarnos/aburrirnos con canciones siniestras por whatsapp; Albena, te iré a ver a Sofia asap; Priscila, qué bien que pasásemos de decir miau por los pasillos del IMM a hacerlo en cenas, exposiciones y demás; Gema, está muy bien eso de tener una antropóloga con ambiciones artísticas en tu vida, le da caché; Fani, nos llevamos aguantando ya una década; Sreb, eres simplemente genial y es un lujo tener a alguien con quien compartir sueños locos; Ana y Héctor, Héctor y Ana...Para empezar, sois como la onda-corpúsculo de De Broglie (Ana la onda y Héctor el corpúsculo, claro). Y lo que la carrera, el gochismo, el humor, la buena literatura y el amor por las películas horteras de los 90, Liam Neeson tras morir su esposa y Adam Sandler han unido, ¡que no lo desuna el hombre!

Y para terminar, esta tesis está dedicada a Ok Hee, la persona con mayor m-index (mother-index) del mundo. Gracias por haberme educado atea, apatriótica y apolítica. Gracias por inculcarme el gusto por la literatura, el cine y el arte. Me ha permitido elegir con mayor libertad intelectual en qué creer y en qué no y a quién escuchar y a quién no.

General index

Resumen y motivación de la tesis

Durante las pasadas décadas, la comunidad científica ha enfocado su interés en el desarrollo de nanoestructuras y nanodispositivos, ya que los materiales presentan nuevas propiedades eléctricas, ópticas, mecánicas y magnéticas a escala nano como consecuencia de la reducción en sus dimensiones y la maximización de su relación superficie/volumen. Dicho desarrollo requiere la disponibilidad de técnicas litográficas precisas capaces de fabricar nanodispositivos con respuestas estables y de manera reproducible. La nanolitografía de microscopía de fuerzas (SPL) pertenece a una de estas técnicas, que comenzó a desarrollarse poco después de la invención del microscopio atómico de fuerzas (AFM), a principios de los noventa. El hecho de que sea una litografía de procesamiento secuencial limita la capacidad de producción tecnológica, pero ofrece varias ventajas interesantes de cara a la fabricación de dispositivos nanométricos a nivel académico:

- El AFM se puede usar como la misma herramienta para fabricar motivos, monitorizar el proceso durante la fabricación e inspeccionar los motivos fabricados justo después.

- El proceso de fabricación se puede llevar a cabo bajo condiciones ambiente y sin necesidad de recurrir a montajes experimentales complejos.

- Se pueden fabricar motivos con diferentes geometrías y controlar su posicionamiento en áreas localizadas con precisión nanométrica. Como consecuencia, es una técnica fácil de integrar en procesos top-down.

- Se pueden fabricar motivos en una gran variedad de materiales de distintas naturalezas: metales, semiconductores, polímeros, monocapas autoensambladas y muestras biológicas.

- Se puede variar la química del proceso de fabricación trabajando con distintos medios como vapor de agua, vapores orgánicos y soluciones.

En el grupo de investigación donde se ha desarrollado esta tesis ha habido una actividad continua explorando el potencial de la nanolitografía de microscopía de fuerzas, en concreto la nanolitografía de oxidación local, encaminada hacia su establecimiento como una litografía de rutina para la fabricación de nanodispositivos con buena resolución (10-50 nm) y reproducibilidad. Algunas de las contribuciones clave del grupo fueron:

- Un estudio detallado sobre el rol que ejerce el menisco de agua en el proceso de oxidación y el campo eléctrico necesario para formar dicho menisco cuando se lleva a cabo el SPL en modo dinámico [1].

- Demostrar que el SPL en modo dinámico proporciona los motivos nanométricos con la mejor resolución, relación altura/anchura y reproducibilidad y ser uno de los grupos pioneros en fabricar motivos mediante nanolitografía por AFM en un medio distinto al del vapor de agua [2].

- Desarrollar la nanolitografía de oxidación local en paralelo como una posible estrategia para superar las limitaciones tecnológicas de la técnica [3].

- Conseguir los patrones basados en ordenamiento molecular y el dispositivo basado en nanohilos de silicio con la mejor resolución fabricados por SPL hasta la fecha [4].

- El uso de transistores de efecto campo basados en nanohilos de silicio fabricados mediante la nanolitografía de microscopía de fuerzas como biosensores para el seguimiento de procesos de reconocimiento molecular [5].

Los dos últimos logros descritos constituyen una prueba de concepto para demostrar las aptitudes de la nanolitografía de oxidación local para fabricar nanodispositivos funcionales, al menos con fines académicos. Sin embargo, el uso de estos dispositivos en aplicaciones específicas, por ejemplo, el biosensor citado anteriormente, requiere tener un buen conocimiento de sus propiedades eléctricas, optimizar el funcionamiento de los dispositivos y el desarrollo de un método de transferencia de patrones reproducible y preciso. En este sentido, el trabajo desarrollado en la presente tesis se ha centrado en realizar progresos hacia la integración de la nanolitografía de oxidación local en el procesamiento top-down para la fabricación de dispositivos, y hacia la búsqueda de nuevas posibles aplicaciones para explotar dichos dispositivos.

El manuscrito se divide en cinco capítulos y las conclusiones generales. Su contenido está descrito a continuación:

- El capítulo 1 proporciona un repaso sobre las distintas familias de nanolitografía de microscopía de fuerzas existentes y un repaso detallado del trabajo desarrollado en la nanolitografía por oxidación local hasta la actualidad.

- El capítulo 2 describe el montaje experimental y la fabricación de motivos por oxidación local relacionados con esta tesis.

- El capítulo 3 describe el proceso de fabricación de transistores basados en nanohilos de silicio por oxidación local, la optimización de las propiedades eléctricas de los dispositivos mediante tratamiento térmico (RTA), la caracterización de sus características como transistores y la comparación de dichas propiedades eléctricas con las de otros dispositivos similares fabricados por litografía de haces de electrones (EBL).

- El capítulo 4 describe la utilización de un nuevo sustrato de silicio sobre aislante (SOI) con una capa de silicio activo de 12 nm de espesor y una capa de óxido de silicio de 25 nm de espesor para la fabricación de transistores basados en nanohilos de silicio con menor tamaño y mejores características eléctricas. Se ha optimizado un proceso de ataque seco (RIE) para producir nanohilos de silicio con 12 nm de espesor usando máscaras de óxido de silicio de 1 nm de altura. Sin embargo, aún no se ha logrado dispositivos que conduzcan. Los próximos pasos hacia la obtención de dispositivos que funcionen son descritos al final del capítulo.

- El capítulo 5 describe dos ejemplos concretos de aplicaciones de la nanolitografía de microscopía de fuerza: el uso de los transistores basados en nanohilos de silicio fabricados por oxidación local decorados con nanopartículas de oro como fotodetectores selectivos y la fabricación de transistores basados en películas delgadas de MoS_2.

- Al final, se dan las conclusiones generales sobre la tesis.

Summary and outlook of the thesis

During the last decades, the scientific research has focused its interest on the development of nano patterns and nano devices, since the materials in this scale present new electrical, optical, mechanical and magnetic properties as a consequence of the reduction of their size and the maximization of their surface/volume ratio. This requires the availability of precise lithography methods which are able to fabricate such structures with reproducibility and stable response. Scanning probe lithography (SPL) is one of these techniques, which started to be developed few years after the invention of the atomic force microscope (AFM), in the early 90s. Serial processing and relatively low throughput pose important limitations, but SPL offers several appealing features such as:

- The ability to use the AFM as the same tool to fabricate patterns, to monitor the process during the patterning and to inspect the created features by imaging after finishing the lithographic process.

- The ability to carry out the fabrication process under ambient conditions and without expensive/complicate set-up requirements.

- The ability to make patterns with many different shapes and control the positioning of these patterns in small, localized areas. As a consequence, its ease of integration in top-down processing.

- The ability to make patterns in many different materials: metals, semiconductors, polymers, self-assembled monolayers, biological samples.

- The ability to tune the chemistry of the fabrication process working in different media such as air with controlled relative humidity, organic vapor, or in solutions.

In the group where this thesis has been developed, there has been a continuous activity to move from the potential of oxidation scanning probe lithography (o-SPL) to the establishment of the technique as a routine lithography to make working nano devices with good resolution (10-50 nm) and reproducibility. Some of the key contributions in o-SPL from this group have been:

- An in depth study of the water meniscus role in o-SPL and the electric field needed to form it in amplitude modulation mode [1].

- To demonstrate that o-SPL performed in amplitude modulation mode gives the features with best resolution, height/width ratio and reproducibility and being one of the first groups which addressed the use of other media than water to perform the oxidation with an AFM [2].

- To carry out a strategy to overcome the slowness of the fabrication process and increase the throughput of the technique by the development of parallel local oxidation nanolithography [3].

- To achieve the template growth patterning and the fabrication of silicon nanowire field effect transistors (SiNW FETs) by o-SPL with the best resolution up to now [4].

- To use o-SPL fabricated SiNW FETs as free-label biosensors in molecular recognition processes [5].

The last two achievements constitute a proof-of concept for the suitability of o-SPL to fabricate interesting functional nano devices, at least for academic research purposes. However, to use these devices in specific applications, for example, the SiNW FETs as free-label biosensors requires having a good knowledge of their electrical properties, to optimize the performance of the devices and to have a reliable pattern transfer method, as it is required for any other device made by any other lithography. In this sense, the work developed in this thesis has been devoted to make some progress towards the integration of oxidation scanning probe lithography in top-down processing for the fabrication of devices and to keep on searching for new possible applications to exploit these devices. The manuscript is divided into 5 chapters and the general conclusions. Its content is described below:

- Chapter 1 gives an overview of the different scanning probe lithography families and a detailed overview of the work developed in oxidation scanning probe lithography up to now.

- Chapter 2 focuses on the o-SPL experimental set-up and the patterning results related to this thesis.

- Chapter 3 gives a description of the fabrication process of SiNW FETs by o-SPL, the optimization of their electrical properties by rapid thermal annealing (RTA), the characterization of their transistor characteristics, and a comparison of their electrical properties with the electrical properties of similar SiNW FETs fabricated by electron beam lithography (EBL).

- Chapter 4 describes the work on progress in the use of a new silicon on insulator substrate with 12 nm and 25 nm thickness of p-type Si (100) layer and buried oxide (BOX), respectively, as a strategy to fabricate o-SPL SiNW FETs with smaller size and subtreshold swing. The optimization of the reactive ion etching (RIE) step to get a reliable and precise pattern transfer from a very thin oxide o-SPL mask of 1 nm thick onto the 12 nm thickness of the silicon layer has been accomplished. However, working devices have not been obtained yet. The next steps towards the production of conductive nanowire transistors are described.

- Chapter 5 describes the work on progress in the integration of oxidation scanning probe lithography in two concrete applications: Hybrid nanoparticle-nanowire photodetectors and MoS_2 thin layer field effect transistors.

- At the end, the main conclusions of the work done during this thesis are described.

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Acronyms

AFM: *Atomic Force Microscopy*

AM-AFM: *Amplitude Modulation Atomic Force Microscopy*

b-SPL: *biased-induced Scanning Probe Lithography*

BOX: *Buried Oxide*

CCP: *Capacitively Coupled Plasma*

CMOS: *Complementary Metal Oxide Semiconductor*

CTAB-Au NPs: *Cetyltrimethylammonium bromide coated gold nanoparticles*

CVD: *Chemical Vapor Deposition*

DPN: *Dip Pen Nanolithography*

EBL: *Electron Beam Lithography*

FET: *Field Effect Transistor*

FIB: *Focused Ion Beam*

FM-AFM: *Frequency Modulation Atomic Force Microscopy*

FWHM: *Full Width at Half Maximum*

LAO: *Local Anodic Oxidation*

LON: *Local Oxidation Nanolithography*

LPCVD: *Low Pressure Chemical Vapor Deposition*

m-SPL: *mechanical Scanning Probe Lithography*

MHA: *16-mercaptohexadecanoic acid*

NEMS: *Nanoelectromechanical systems*

NIL: *Nano Imprint Lithography*

NPs: *nanoparticles*

o-SPL: *oxidation Scanning Probe Lithography*

OTS: *n-octadecyltrichlorosilane, CH_3-$(CH_2)_{17}$-$SiCl_3$*

PSPD: *Position Sensitive Photodiode*

Redox: *reduction-oxidation reaction*

rf-power: *radiofrequency power*

RIE: *Reactive Ion Etching*

RH: *Relative Humidity*

RTA: *Rapid Thermal Annealing*

SAM: *Self-Assembled Monolayer*

SB-FET: *Schottky Barrier Field Effect Transistor*

SEM: *Scanning Electron Microscope*

SIMOX: *Separation by Implantation of Oxygen*

SiNW: *silicon nanowire*

SNAP: *Superlattice Nanowire Pattern Transfer*

SOI: *Silicon on Insulator*

SPL: *Scanning Probe Lithography*

SS: *Subthreshold Swing (mV/dec)*

STM: *Scanning Tunneling Microscope*

t-SPL: *thermal Scanning Probe Lithography*

tc-SPL: *thermo-chemical Scanning Probe Lithography*

TEM: *Transmission Electron Microscope*

UT-SOI: *Ultra Thin Silicon on Insulator*

VLS: *Vapor-Liquid-Solid synthesis*

Chapter 1

Oxidation Scanning Probe Lithography: Overview of the technique

1.1 The atomic force microscopy

Since its invention in 1986 by Binnig, Quate and Gerber [6], atomic force microscopy has become the most versatile tool to characterize any kind of materials in different ambient, from UHV to liquid. The AFM can be configured to measure magnetic [MFM], electrostatic [KPM] or mechanic properties. The AFM can be used to manipulate atoms [7] and as a lithographic tool to fabricate devices. In its current state of the art, the AFM can achieve atomic resolution [8, 9] and can track topography below surface [10]. Lately, the AFM is being exploited to understand many biological systems such as protein-DNA interaction, antibodies or cancer cells [11-13].

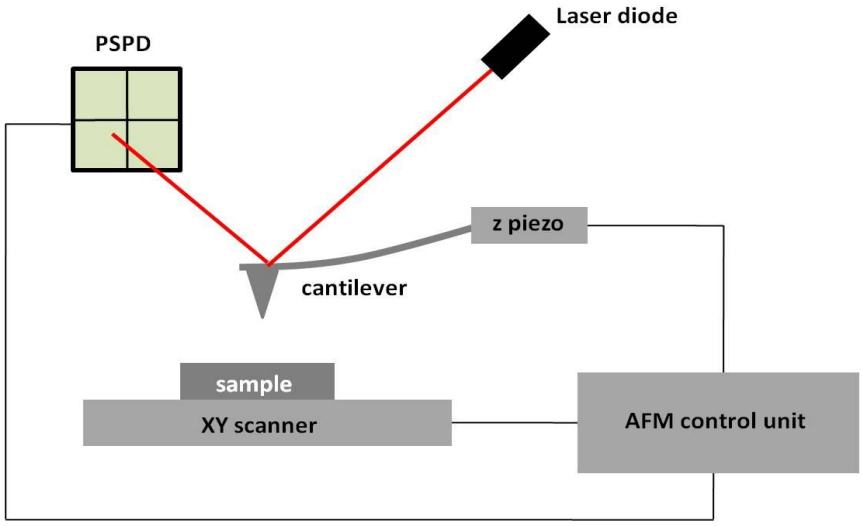

Figure 1.1. Scheme of an atomic force microscopy with its main components.

The principal elements of an AFM are represented in figure 1.1. The **probe** consists in a cantilever with a sharp tip at the free end, normally made of silicon, silicon nitride, or silicon with a metallic coating [14, 15]. As each experiment requires specific conditions in terms of the sample characteristics and the environment where they are measured, the type of cantilever is chosen according to its resonant frequency, f_0, and force constant, k.

Therefore, there are available cantilevers with different geometries, dimensions and materials. A **piezoelectric system** allows the movement in *z* to approach/retract the tip and the movement in *x* and *y* when the tip is scanning over the surface. The samples can be mounted on a piezoelectric scanner that moves in the *xy* plane directions. The movement of the cantilever is tracked by the **beam deflection system** [16]. The reflection of a laser beam from the back side of the cantilever is collected by a position sensitive photodiode (PSPD). The PSPD is a four-segmented detector and measures the movement of the cantilever taking into account the variations on the position of the laser spot. A **close-loop** system corrects the drift caused by the non-linear behavior of the piezoelectric. The microscope and the sample are placed on an **anti vibration table** to minimize the introduction of noise during the acquisition of the images. Depending on the chosen working mode, a **feedback unit** maintains constant the deflection, amplitude or frequency of the cantilever during the scanning. The **control unit** of the AFM processes the signals collected by the detection system. Finally, a computer incorporated with a **software program** is needed for the acquisition and processing of the images.

Regarding the cantilever motion in *z*, the AFM can be operated by several modes separated into two big groups: Contact or static mode and dynamic mode.

- In contact mode (figure 1.2a), the apex of the tip is very close to the surface of the sample and the interaction force between them has a repulsive nature. In this mode, the feedback unit keeps constant the deflection of the cantilever during the scanning. With the contact mode it is possible to achieve high resolution in hard samples and liquid ambient, but the tip wears faster than in dynamic mode due to the continuous mechanical contact.

- In the dynamic mode (figure 1.2b), the tip oscillates over the surface of the sample with a determined amplitude and frequency [17]. When the tip approaches to the surface, the interaction forces between them change the original oscillation amplitude and frequency. If the AFM works in the amplitude modulation mode (AM-AFM), the feedback will stretch or retract the piezoelectric until the cantilever recovers the initial amplitude. In frequency modulation mode (FM-AFM), the change in the resonant frequency (Δf) is used as the feedback parameter. Normally, AM-AFM is performed in air or liquid and allows extracting topographic and compositional information simultaneously. On the other hand, FM-AFM is used to measure atomic resolution in ultra high vacuum (UHV).

- During the last years, a new mode which exploits the different eigenmodes of the cantilever oscillation, called multifrequency, has emerged. It is pushing the limits of resolution and compositional information achievable with the atomic force microscopy [18]. In particular, in the bimodal mode, two different driving forces are applied to excite the oscillation of the cantilever. Then, the motion of the tip is expressed as:

$$z = z_0 + q_1(t) + q_2(t) = z_0 + A_1 \cos(\omega_1 t - \phi_1) + A_2 \cos(\omega_2 t - \phi_2) \quad (1.1)$$

Where:

- z_0 is the static component of the deflection.
- q_j, j=1, 2; represents the two eigenmodes.
- A_j and ϕ_j, j =1, 2; are the amplitudes and phase shifts of the two excited modes, respectively.

The user choses the amplitude or the frequency shift of the first mode as the output signal to obtain topographical mapping and the amplitude or the frequency shift of the second mode as the output signal to extract information about a specific property of the surface material, for instance, the mechanical compliance. One of the strengths of the bimodal AFM is that allows the operation of the microscope at very low forces, in the order of pN, making it useful to characterize biological samples.

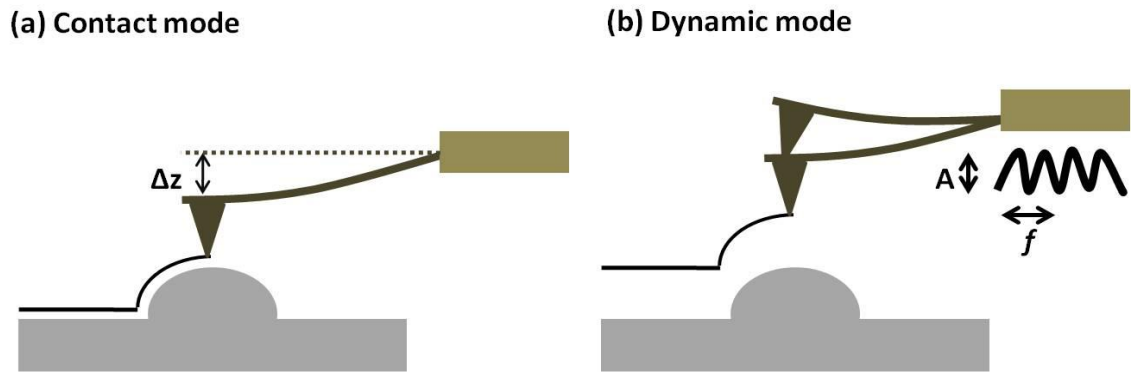

Figure 1.2. (a) AFM operating in contact or static mode. (b) AFM operating in dynamic mode.

In this thesis, both the patterning and the imaging of the fabricated nanostructures are performed with the AFM working in AM-AFM.

In AM-AFM there are two regimes of operation as a function of the free amplitude: repulsive and attractive mode; and a zone of instability where coexist two possible oscillation states of the cantilever [19, 20]. This can be seen in the equation of motion of the cantilever-tip system considered as a forced harmonic oscillator with damping, approaching the cantilever-tip system as a point-mass spring:

$$m\ddot{z} = -kz - \frac{m\omega_0}{Q} + F_0 \cos(\omega t) + F_{ts} \quad (1.2)$$

Where:

- From the driving force, F_0 and ω are the amplitude and angular frequency, respectively.
- From the cantilever, Q, ω_0 and k are the quality factor, angular resonance frequency and force constant of the free cantilever, respectively. The quality factor Q of an oscillator is defined as the ratio between the stored energy and the energy dissipated with the media per cycle:

$$Q = \pi \frac{E_{stored}}{E_{dissipated}} \approx \frac{\omega_0}{\Delta\omega} \qquad (1.3)$$

  Hence, the term -m ω_0/Q is related to the damping forces.
- F_{ts} encompasses the tip-surface interaction forces.

Equation (1.2) is a non-linear, second-order differential equation. It could have two possible solutions: One corresponds to the high amplitude state, where the predominant interactions are repulsive forces and there will be contact between the tip and the sample. The other corresponds to the low amplitude state, where the main interactions are attractive forces and there will not be contact between the tip and the sample. Therefore, depending on the type of sample, the user can chose to operate the AFM without contact between the tip and the sample or with the tip contacting the surface at the end of each oscillation. For example, to imaging soft matter such as biological samples, it is better to work in the low amplitude state, since the application of smaller forces reduces the damage of the sample. On the other hand, it is possible to obtain better compositional contrast with hard heterogeneous samples working in the high amplitude state, as the dissipation energy on the sample is usually related to the repulsive regime. The bistable region has to be avoided because the images are noisy in this region, due to the fact that any perturbation could change the oscillation regime of the cantilever. The election of the free amplitude and the working regimes can be done by checking experimentally the force curves (figure 1.3).

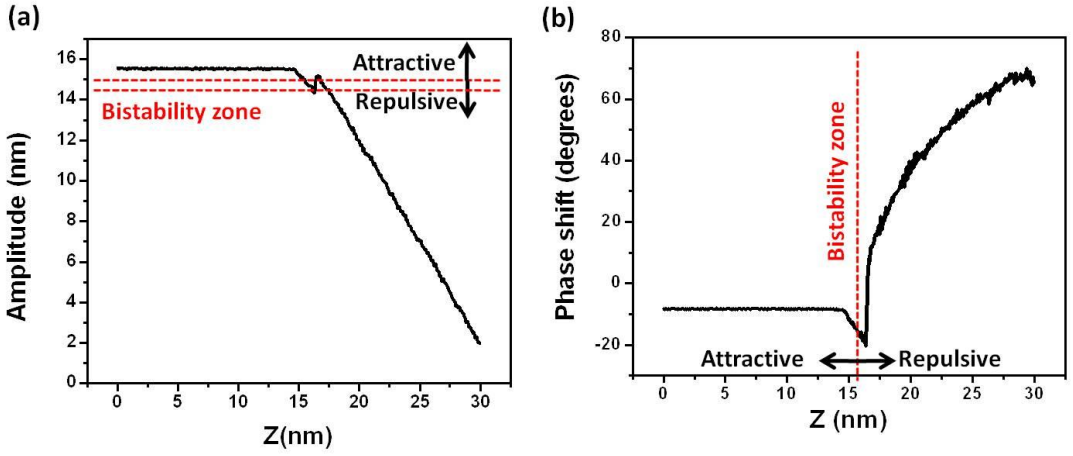

Figure 1.3. Force curves in dynamic mode: (a) Amplitud vs z, (b) Phase shift vs z. The region located between the red dotted lines in (a) is noisy and has to be avoided to take images.

In AM-AFM, besides the topography image, from which the width and the height of the objects can be measured, it is also possible to obtain compositional contrast from the phase image [21]. The phase image is extracted from the phase-shift lag ϕ between the external driving excitation and the cantilever response:

$$\sin\phi = \frac{A}{A_0}\left(1+\frac{E_{dis}}{E_{med}}\right) \qquad (1.4)$$

Where:

- A_0 is the free amplitude.
- E_{med} is the average energy which the cantilever releases to the medium.
- E_{dis} is the average dissipation energy released from the sample.

As A, A_0 and E_{med} remain constant during the surface scanning in the AM mode, the phase-shift lag ϕ will be related to the dissipation energy. This dissipation energy is different for each material. Therefore, if a surface with different components is analyzed, the phase image will show contrast among them.

1.2 The atomic force microscopy as a tool for lithography.

All the scanning probe lithography (SPL) techniques are based on the use of an SPM tip to modify locally a surface by depositing, removing or growing material on it with nanometric precision. The first patterning experiments using a scanning probe microscope (SPM) were carried out with scanning tunneling microscopes (STM) [22 - 25] and they are still being used in some fabrication processes. However, currently, the atomic force microscope is the tool of choice to perform scanning probe lithography. In this section, only the work developed in scanning probe lithography with an AFM will be considered.

It is not easy to have a neat classification of the different SPL techniques because most of them involve a combination of chemical and physical mechanisms. For example, oxidation SPL is a variant of bias-induced SPL where the bias activates an anodic oxidation process, but it is normally considered as a whole branch of SPL. Taking into account the main type of interaction employed to modify the surface of the material, they can be divided into [26]:

- Mechanical SPL (m-SPL): It is the simplest approach of scanning probe lithography and it involves physical mechanisms exclusively. It is an analogue to indentation/scratching processes in the nanoscale. In this case, the tip is used to remove selectively the material from a solid surface or from layers of functionalized substrates [27, 28]. In particular, nanoshaving [29] consists in the local displacement of molecules from a self-assembled monolayer (SAM). In the case of nanografting [30], the spaces left after the local removal of molecules from

the SAM layer over a surface are refilled with other molecules forming patterns of a different SAM.

- Bias-induced SPL (b-SPL): The electron current of the high electric field between the tip and the sample is used to decompose locally molecules of a gas or a solution that are deposited on the surface forming patterns of a new material or to desorb molecules from the functionalized surface to define the patterns [31-36]. The most developed and used technique of the b-SPL is oxidation scanning probe lithography (o-SPL), also called local oxidation nanolithography (LON) or local anodic oxidation (LAO). Being the technique employed in this thesis, it will be fully explained in the next sections.

- Dip-Pen Nanolithography (DPN): In this technique, the direct writing of patterns is produced by virtue of the transport of molecules from an AFM tip wetted with a solution that contains those molecules to a surface [37, 38]. As a non-destructive technique compatible with soft-matter, DPN has been used to fabricate 16-mercaptohexadecanoic acid (MHA) nanodots as templates for anti-p24 antibody immobilization, to study the binding events of these antibodies with HIV-1 p24 antigens with the AFM [39].

- Thermal SPL (t-SPL): A probe with a special design is used to perform the experiments. It consists in highly doped cantilever legs and a low-doped region where the tip is located. The tip is heated resistively when a current is passed by the cantilever legs. This 'hot' tip is used to change locally the properties of a molecular resist and then, to remove the changed material. By this way, the tip is used to write the patterns [40 - 42]. In this technique, the tip is heated to write the patterns. Some of the applications of thermal SPL include data storage [43], 3D-patterning [44 - 46] and pattern transfer [47].

- Thermo-chemical SPL (tc-SPL): This technique is similar to t-SPL. It also uses hot tips to make the modifications but in this case, the temperature of the tip is employed to trigger chemical reactions in a precursor material, obtaining a pattern with a different composition and structure [48]. Examples of the tc-SPL as a tool to fabricate devices by controlling very local chemical reactions are reduced graphene oxide nanoribbons [49], pentacene field-effect transistors [50] and templates for functional nano patterns [51].

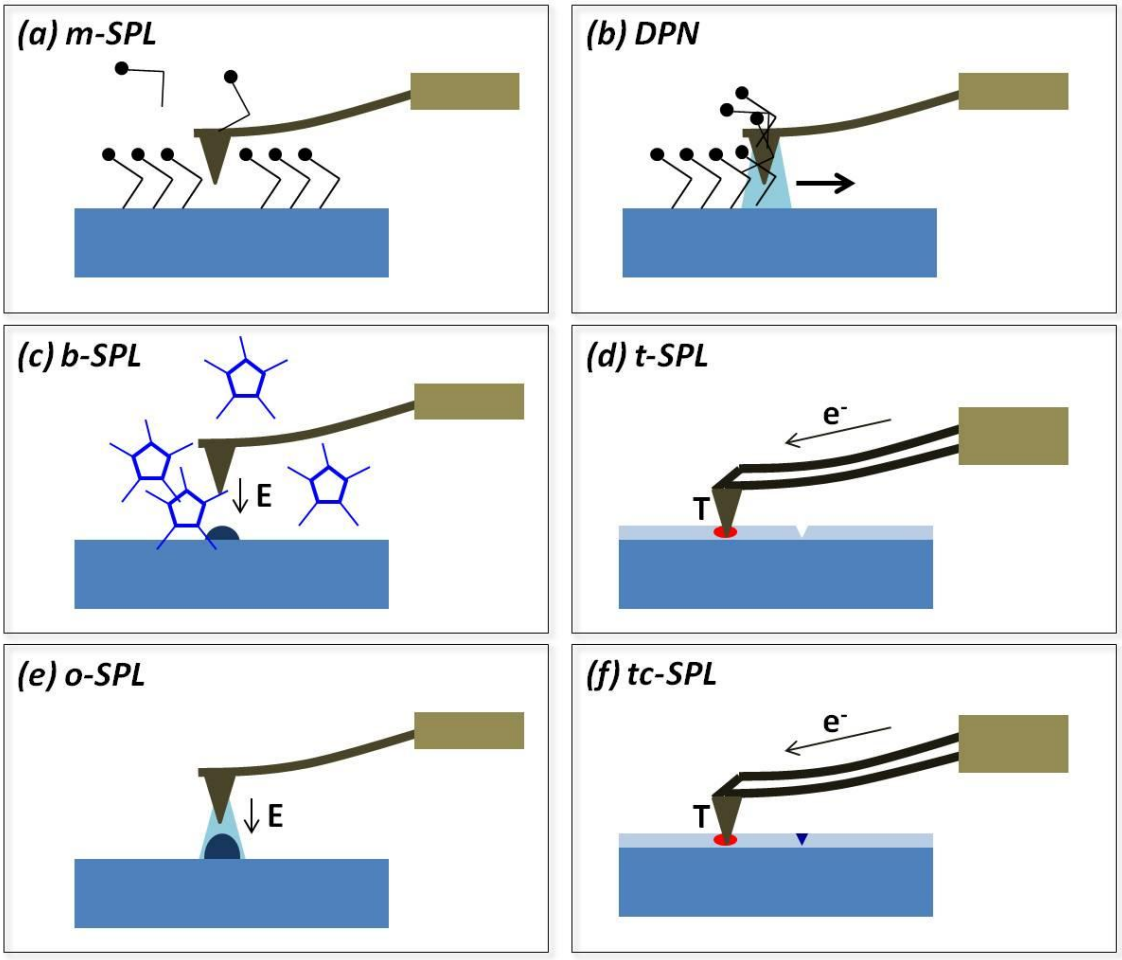

Figure 1.4. Scheme of the different SPL techniques: (a) Mechanical SPL. The molecules of a self-assembled monolayer which covers a surface are removed selectively by the tip. (b) Dip Pen nanolithography. The tip, wetted with a solution that contains molecules, acts as a 'pen' delivering the molecules to a surface. (c) Bias SPL. The high electric field (***E***) concentrated between the tip and the surface is used to decompose molecules of a gas or a solution that are deposited on the surface forming patterns of a new material. (d) Thermal SPL. The patterns are created by changing the properties of a molecular resist and removing the changed material with a heated tip. (e) Oxidation SPL. The ***E*** between the tip and the sample forms a water meniscus within which a redox reaction occurs, oxidizing locally the surface of different materials. (f) Thermo-chemical SPL. In this case, the heated tip is employed to trigger chemical reactions in a precursor material.

1.3 Oxidation scanning probe lithography

An SPM tip was used as an oxidation tool for the first time by Dagata and coworkers in 1990 [25]. In this work, an STM tip operating in air was employed to make modifications on a hydrogen-passivated (111) silicon surface. Then, in 1993, Day and Allee [52] reported the use of an AFM to perform the oxidations with a metalized silicon nitride tip. They considered the advantage of using an AFM over a STM due to the capability of the first to decouple the tip voltage and current from the tip sample spacing [53] to enhance

the reproducibility and make oxide lines. Sugimura et Nakagiri [54] were the first that addressed the role of the adsorbed water layer as the responsible of the anodization process and pointed out the influence of the relative humidity in the thickness of this water layer and consequently, in the size of the oxides. Also in this work, the SPL oxides were used for the first time with pattern transfer purposes, by wet etching. Soon after, the potential of the technique as a lithographic tool to make devices was proved by Snow and Campbell [55, 56]. Since then, there has been a continuous effort in the oxidation scanning probe lithography field to understand the mechanism and the kinetics involved in the process, to optimize the patterning parameters to improve the resolution and reproducibillty, to explore new materials where the technique can be applied and to make small and functional nano devices.

1.3.1 Mechanism

The water meniscus formed between the tip and the surface acts as an electrochemical nanocell. When a relatively mild voltage is applied, in the range of 10-30 V, as the distance between the tip and the sample is of few nanometers, a very high electric field is created, in the order of 10^9-10^{10} V/nm. This field is able to dissociate the water molecules of the meniscus into the oxyanion species that are needed to oxidize the silicon surface. With the right polarity, the tip biased negatively with respect to the sample, the reduction-oxidation (redox) reaction that takes place inside the water meniscus is:

$$Si + 4OH^- + 4h^+ \rightarrow SiO_2 + 2H_2O \qquad \text{Anodic semi reaction (1.5)}$$

$$2H^+ + 2e^- \rightarrow H_2 \qquad \text{Cathodic semi reaction (1.6)}$$

The anodic reaction, equation (1.5), occurs at the meniscus/surface interface, where the oxide features are created. The reduction of hydrogen, equation (1.6), takes place at the meniscus/tip interface. The faradaic current associated to the flux of the O^- and OH^- ions between the tip and the sample during the redox process has been measured experimentally and it is found to be in the order of sub-picoampers [57].

The water meniscus has another key role in o-SPL: It confines laterally the reaction. This means that the minimum achievable size of a stable meniscus will determine the minimum size of an oxide feature, i.e., the size of the meniscus will give the limit in the lateral resolution of this lithography.

Oxidation SPL has a self-limited growth behavior due to the buildup of space charge during the process [58-62]. In the initial stage of the reaction, the oxide grows fast with the OH^- ions supplied by the external electric field, but for longer oxidation time, the apparition of positive charged defects at the silicon surface while the oxide is forming decreases the effective electric field and thus the oxidation velocity. Chiesa and Garcia [63] have observed that if the oxidation time is short enough, the unreacted OH^- ions give rise to a negative residual space charge.

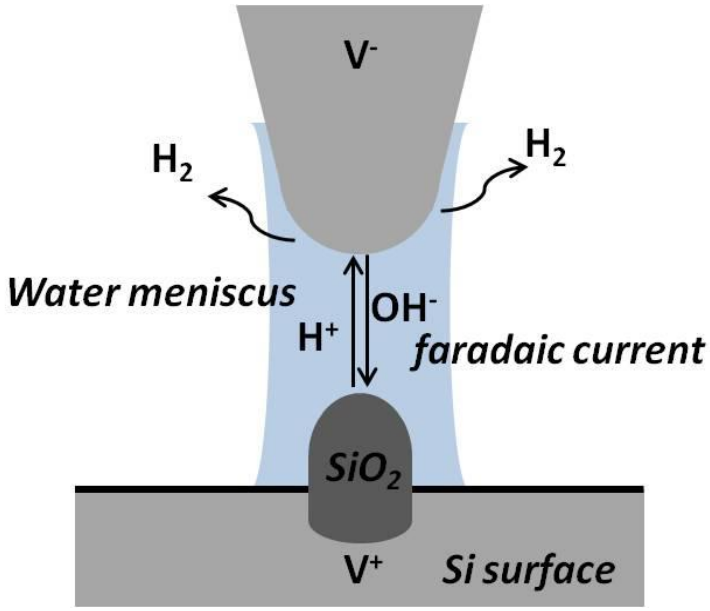

Figure 1.5. Scheme of the redox process which takes place within the water meniscus, formed by means of an electric field in the order of 10^{9}-10^{10} V/nm.

1.3.2 Kinetics

The starting point to build a kinetic model of the local oxidation process was to consider the diffusive model of oxidation on metallic and semiconductor surfaces by Cabrera and Mott [64]. According to this model, due to the applied electric field, the oxyanions of an electrolyte are able to overcome several potential barriers and to incorporate into the surface forming the oxide. This model gives a logarithmic relationship between the height of the oxide and the oxidation time:

$$\frac{h_1}{h} = \ln\left(\frac{h_1 u t}{h_L^2}\right) \qquad (1.7)$$

Where:

- h_1 (V) ~ 10^{-6}-10^{-5} cm.
- $u = u_0 \exp(-W/kT) \sim 10^{4}$ cm/s.
- h_L is a critical height above which the oxide stops growing and is found to be about 10 nm for o-SPL [65].
- W is the energy barrier that an ion has to overcome to go from one interstitial position to another.

However, the experimental data of several groups [65-73] showed that the height of the oxide does not fit to a logarithmic law, but a power law instead. Teuschler *et al* [66] gave

the empirical expression of the power law that is closest to fit the o-SPL experimental data from different groups up to now:

$$h(t) \propto bt^{\gamma} \qquad (1.8)$$

Where b is a constant which depends on the doping of the Si surface and the experimental conditions. The factor γ has a range of 0.12 to 0.4.

Dagata and coworkers [73] proposed a model which explains the empirical power law (equation 1.8) given by Teuschler *et al* and which fits quite well with the available experimental data. According to this model, during the local oxidation process, there exists a competition between two different reactions:

- A direct reaction (A→ C):

$$Si + h^{+} + 2OH^{-} \rightarrow SiO_2 + 2H^{+} \qquad (1.9)$$

- An indirect reaction (A→B→C):

$$H^{+} + OH^{-} \rightarrow H_2O \qquad (1.10)$$

$$H - Si \equiv Si_3 + H_2O + h^{+} \rightarrow {}^{*}Si \equiv Si_3 + H_3O^{+} \qquad (1.11)$$

$$H_3O^{+} + OH^{-} \rightarrow [H_3O^{+} - OH] \qquad (1.12)$$

$$Si + h^{+}[H_3O^{+} - OH] \rightarrow SiO_2 + 2H^{+} \qquad (1.13)$$

Where:

- A is related to the initial concentration of oxyanions.
- B describes the density of fixed charge traps at the forming Si/oxide interface.
- C is the created o-SPL oxide.

The o-SPL oxide has a non-linear dependence with time. At the initial stage of the process, the oxide grows fast due to the reaction of OH^- ions provided by the external electric field with the silicon surface. This corresponds to the direct reaction domain (equation 1.9) and the γ that fits h(t) is about 0.4. For longer oxidation times, the indirect

reaction (equations 1.10-1.13) dominates due to the increase of fixed charge traps in the bulk Si/ o-SPL oxide interface, and a slow growth steady state rate of $h(t) \sim t^{0.2}$ is reached.

1.3.3 Contact vs amplitude modulation o-SPL

The main differences between contact mode and amplitude modulation o-SPL are:

- In the contact mode, water meniscus forms instantaneously when the tip and the sample bring into contact, while in amplitude modulation mode, an electric field is needed to create the meniscus.

- The amplitude modulation mode introduces a new parameter in the o-SPL process, the tip-sample distance.

- In the amplitude modulation mode, the tip is oscillating during the application of the pulse, thus, during the oxidation process.

Garcia's group has performed several studies to characterize the water bridge formed in the AM o-SPL, since the meniscus plays a fundamental role in the reproducibility and the resolution achievable with the technique:

- The experimental estimation of the critical electric field required to form the meniscus, of about 1.3 V/nm, as the ratio of the threshold voltage and the tip-sample distance (D) [74]:

$$E_C = \frac{V_{th}}{D} \qquad (1.14)$$

The threshold voltage to form the bridge and the voltage to growth the oxide are different.

- The experimental estimation of the size of the meniscus in the range of 5-30 nm from the snap-off separation [75].

- The calculation of an expression where the threshold voltage to form the meniscus is given as a function of the relative humidity and the tip-sample distance, taking into consideration the interaction among the field-induced polarization of the adsorbed water layer on the surface, the surface energy and the water condensation from the ambient [76].

Up to now, both contact mode and amplitude modulation mode are used to perform o-SPL, although the amplitude modulation mode o-SPL presents several advantages with respect to the contact mode o-SPL [74-81]:

- In the amplitude modulation mode o-SPL, it is possible to control the separation between the tip and the sample, which in turn controls the diameter of the

meniscus, while in contact o-SPL this is not available. This means that AM o-SPL can offer a better resolution in the lateral size.

- Under similar experimental conditions, the height of the oxides in contact mode o-SPL is always smaller than in AM o-SPL. Tello and Garcia [78] addressed that the vertical growth rate of the oxides in contact mode is smaller due to the mechanical work that the oxide has to exert against the cantilever to keep on growing.

- The effect of lateral forces in contact mode o-SPL leads to a fast wear of the tip, degrading the reproducibility and the resolution of the features. Amplitude modulation o-SPL offer longer tip lifetimes.

- In amplitude modulation mode, the AFM parameters to fabricate the oxides and to take images after the lithography process can be similar.

In conclusion, amplitude modulation o-SPL can give features with smaller lateral size decreasing the diameter of the meniscus and produces higher oxides, so patterning under this AFM mode gives features with the best height/width ratios.

1.3.4 Variables in the performance of o-SPL

All the parameters found in the literature which influence the height, width or height/width ratio of the oxide patterns are listed below:

- **Voltage**: The dependence of the feature size of the oxides with the applied voltage is observed to be linear from the different experimental data when the height or the width of the oxide is represented as a function of the pulse voltage [82-85]. This means that the larger the applied voltage, the larger the oxides in both vertical and lateral directions. The average voltage values range from 10 V to 40 V.

- **AC/DC voltage mode**: The application of voltage waveforms instead of a continuous pulse has been proposed to limit the space charge built up [86 - 88].

- **Oxidation time**: The dependence of the feature size on the oxidation time is smaller than on the applied voltage, when the rest of parameters are fixed. Sometimes, the oxidation time is given by the tip velocity, which experimentally is in the range of μm/s – mm/s. Many empirical results are available in the literature [69-70, 73, 77-78].

- **Relative humidity**: The relative humidity is an important parameter to control the lateral size of the features. The higher the relative humidity, the bigger is the

formed water meniscus and there is more OH available for the oxidation [89, 90], so in general, there is a linear dependence of the relative humidity on the width of the oxides.

- The wetting behavior of the substrate surface, i.e., its **hydrophilicity/hydrophilicity** has shown to influence the level of confinement of the meniscus at a given relative humidity [91, 92].

- **Tip-sample distance/oscillation amplitude**: In the AM o-SPL mode, as it was explained in the previous section, once the meniscus is formed, the ability of getting the largest tip-surface separation while maintaining the stability of the water bridge during the oxidation process will generate smaller oxides in width.

- **Doping of the silicon substrate**: This parameter has an influence on the oxidation growth rate. Specifically, it has been shown that the *p*-doped substrates give a faster growth rate in the vertical direction because the holes on the silicon surface facilitate the reaction with the anionic species favoring the oxidation reaction [66, 93]. Morimoto *et al* [94] also reported the influence of the substrate doping in the oxide density and presented high-resolution cross-sectional transmission electron microscopy images of dislocations in oxides fabricated on *p*-type (100) Si.

- **Crystalline orientation of the silicon**: Fang [95] reported that this parameter has some influence on the oxidation rate, although in o-SPL, the election of the Si crystalline plane is normally determined in function of the application purposes: (100) for microelectronic devices in general and other planes for wet etching [96, 97].

- **AFM probe**: the tip radius and the tip material/ conductivity have influence on the resolution of the features [98] and the oxidation lifetime.

- **The sample conductivity**: Cambel and Soltys [99] have reported that for low-conductive samples the maximum field is located in the edge of the meniscus, in both contact and non-contact mode o-SPL. As a consequence, the widths of the oxides are bigger.

The above parameters are not completely independent among them. For example, the relative humidity should be low to reduce the ionic diffusion and make the width of the oxides smaller. However using a low relative humidity normally requires higher threshold/oxidation voltages. A higher voltage contributes to the lateral diffusion of the ions and thus, to widen the oxide features.

1.3.5 O-SPL on self-assembled monolayers: Constructive Nanolithography

Sagiv's group has developed o-SPL of self assembled monolayers to build molecular architectures [100 - 103]. The technique consists in the selective oxidation of areas of an OTS (n-octadecyltrichlorosilane, CH_3-$(CH_2)_{17}$-$SiCl_3$) monolayer on a Si substrate. This method is called 'constructive nanolithography' because of its additive character. The selective oxidation of OTS into carboxylic acid (COOH) groups serves as a step to define a template to deposit other organic layers. The chemical reactions that take place between the tip and the surface are, being the tip biased negatively with respect to the surface [104]:

At the tip:

$$2H_2O + 2e^- \rightarrow H_2 + 2OH^- \qquad (1.15)$$

At the surface:

$$R - CH_3 + 2OH^- + 2h^+ \rightarrow RCOOH + 2H_2 \qquad (1.16)$$

Depending on the oxidation parameters, two different regimes of patterning exist: For small and short voltage pulses (<8 V, ~1 ms) the oxidation is confined to the functionalized organic monolayer. However, for higher and longer voltage pulses the initial monolayer is totally degraded and the anodization of the underlying Si substrate occurs [105]. The existence of these two regimes has been exploited to generate ring-like structures that have a core made of silicon oxide and a rim made of the SAM molecules [106].

The technique was also applied to pattern mm^2 areas by replacing the AFM tip with a TEM grid which served as a conductive stamp. They called this process 'constructive microlithography' [107, 108]. Recently, Sagiv and coworkers have presented a variation of constructive microlithography to generate metallic micro/nano patterns [109]. In this process, first, a stamp made of a silver film deposited on an OTS/Si substrate is put in contact with a target surface. The target surface is made of an OTS monolayer on Si. This surface was previously patterned by AFM oxidation lithography. Then, by biasing the stamp positively with respect to the target, the silver ions are transferred selectively on the chemically activated –COOH terminals of the oxidized OTS. In this process, the adsorbed water layer acts as an electrolyte.

Constructive nanolithography combines bottom-up and top-down nanofabrication processes and has the potential to generate complex interfaces.

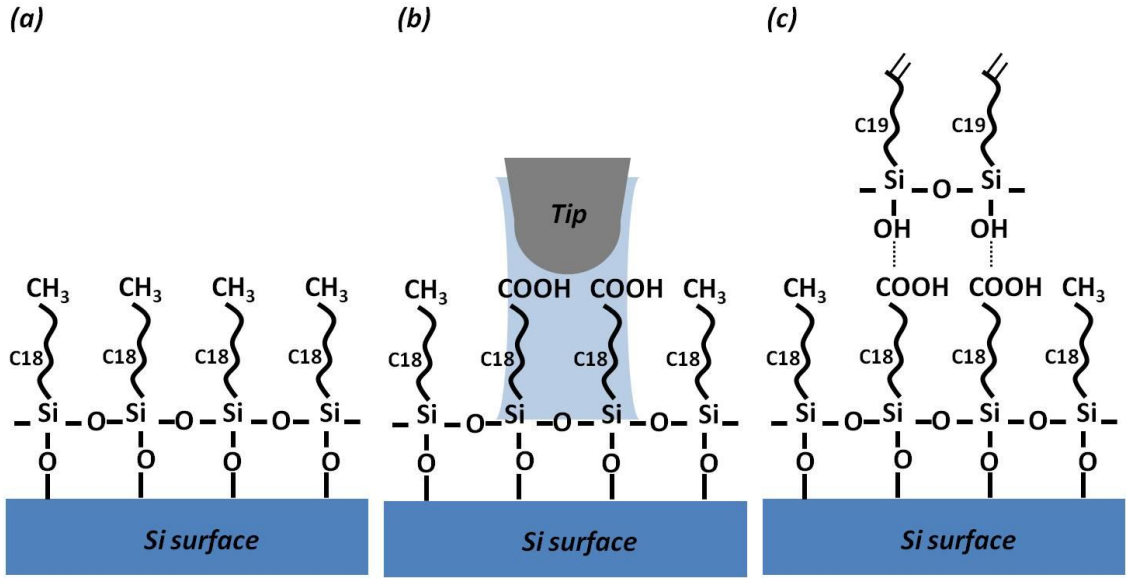

Figure 1.6. Scheme of the constructive nanolithography process. (a) The silicon surface is functionalized with a self-assembled monolayer of OTS. (b) By applying o-SPL, the tip makes selectively patterns of carboxylic acid (COOH) groups. (c) After exposure to a solution of NTS (C19, nonadecenyltrichlorosilane), a new self-assembled monolayer is formed only in the areas which were modified by the AFM tip.

1.3.6 Applications

Oxidation scanning probe lithography has been applied to pattern a broad range of materials and to fabricate a wide variety of devices:

- Materials: Ti [110 - 112], SiC [113, 114], Nb [115], Si_3N_4 [116], Mo [117], ZrN [118], graphene [119 - 121], Cu (II) acetate ($Cu(CH_3COO)_2$) [122], GaAs [123 - 125], Al [126], Ni [127], Ta [128] and as described in the previous section, self-assembled monolayers.
- Template growth/patterning guide [129 - 133].
- Masks for pattern transfer [96 - 97, 134].
- Electronic devices [135-141].
- Optical devices [142, 143].
- Quantum devices [121, 144].
- Memory applications [145, 146].
- Free-label biosensor [5].
- Hybrid SPL mode: Sometimes, it is possible to tune easily from anodic oxidation to solvent decomposition just tuning the surface termination [147] or, using the correct voltage range and polarity under the same organic atmosphere [92].

1.3.7 Chapter summary

The aim of this chapter was to provide a complete review of the fundamentals and applications of oxidation scanning probe lithography. A recap of the strengths and weaknesses of the technique is given below to summarize it.

Among the pros of o-SPL are:

- The same tool is used for lithography and inspection of the fabricated patterns.
- Very good positioning capability.
- The fabrication of structures with arbitrary shapes/overlapped is possible.
- Lithography performed in ambient conditions.
- It is easy to integrate in top-down/CMOS technology.
- It can be applied to almost any kind of materials: semiconductors, metals, polymers or self-assembly monolayers.
- It can be performed under different atmospheres.
- It is a robust lithography that does not require special set-up conditions.
- The reproducibility to fabricate structures with sub-50 nm lateral resolution is very good.

Among the cons of o-SPL are:

- It is slow due to its serial nature.
- The throughput is lower than the achieved by other SPL techniques such as t-SPL and tc-SPL.
- The tip lifetime is limited to thousand of oxides.
- The lateral resolution is limited by kinetics and meniscus size.

Currently, the improvement in the lateral resolution is the most difficult task to achieve in o-SPL. To overcome the issue of slowness, high speed AFM for o-SPL has been proposed [148]. To overcome the issue of low throughput, parallel approaches are being developed [4, 33, 107-109].

Chapter 2

Oxidation scanning probe lithography: Experimental set-up and patterning capabilities

In this thesis, the oxidation experiments were carried out by amplitude modulation o-SPL. The width of the patterns is given by full width at half maximum (HWFM), unless otherwise indicated.

According to the variables to take into account during the performance of o-SPL described in section 1.3.4, the patterns fabricated in this section correspond to:

- Si (100)-oriented (**crystalline plane**).
- *p*-type with a nominal resistivity of about 15 Ω•cm (**doping type** and **conductivity of the sample**).
- **DC voltage mode.**
- **Free amplitude** in the range of 4-10 nm.
- **Voltage** in the range of 12-30 V.
- **Oxidation time** in the range of μs-s.
- **Relative humidity** in the range of 30-60%.
- **Hydrophilic** surface.
- **AFM probe**: n+-doped silicon cantilevers (NCH-W, NanoWorld) with a force constant of about 40 N/m and a resonant frequency about 300 kHz. The nominal radius of the tip is about 10 nm.

2.1 Cleaning of the sample

After cutting the silicon/ silicon on insulator substrates into small pieces by a diamond tip, these substrates have to undergo a cleaning protocol in order to remove the inorganic nanoparticles attached on the surface and the dust created after the cutting. The cleaning protocol is a variant of the classic RCA cleaning and it consists in:

1. Three cycles in a solution of NH_4OH: H_2O_2: DI H_2O (1:1:2), soaking by ultrasound. Each cycle last about 10-12 min. The solution is changed between each cycle.

2. Another cycle of 5 min in DI water is applied to the samples to ensure the elimination of precipitates formed during the previous cycles.

3. Finally, the samples are dried with nitrogen.

After this cleaning protocol, the surface of the silicon gets more hydrophilic, favoring the formation of the water meniscus in the oxidation process by AM-AFM.

If the oxidation comes after a photolithography step, to remove organic contamination, the samples are placed under ultraviolet light to expose them in ozone atmosphere during 10-30 minutes.

2.2 Set-up and oxidation process

The main components of the experimental set-up to perform oxidation scanning probe lithography are shown in figure 2.1. The **AFM** used for the fabrication of the patterns and their characterization is the Dimension V, with the controller Nanoscope V (Vecco). The **sample holder** is connected with a **pulse generator**. The AFM and the sample are isolated by a **chamber** to keep constant the relative humidity during the lithography. Inside the chamber, two inlets connected one to nitrogen and the other to a **flask filled with water** are used to control the relative humidity of the process. The water in the flask is bubbled with nitrogen to carry water vapour into the chamber. The level of relative humidity can be checked by a **hygrometer**. One of the channels of the **oscilloscope** is connected with the pulse generator and a second channel with a home built **single access module** that gives the output signal of the deflection of the cantilever. With these channels, both the application of the pulses and the formation of the meniscus and the oxidation can be monitored during the lithographic process.

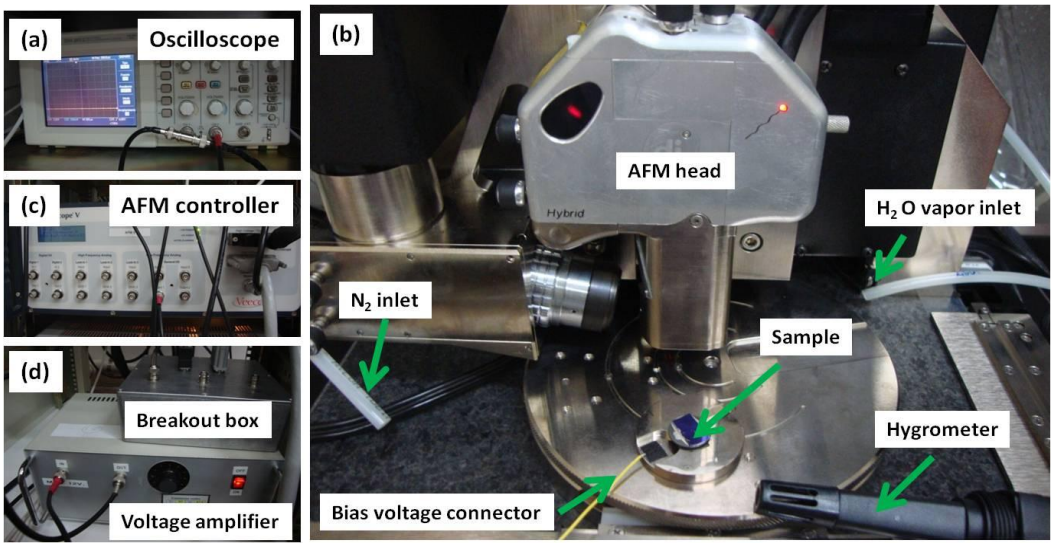

Figure 2.1. Components of the o-SPL experimental set-up. (a) The application of the pulses and the formation of the water meniscus and the oxidation process are monitored in real time by an oscilloscope. (b) o-SPL environment. (c) The AFM controller used for the experiments, Nanoscope V. (d) A home built breakout box allows to have access to the output signal of the cantilever deflection.

The oxidation steps consist in:

1 The pumping of water in the flask by a flux of nitrogen until the desired relative humidity is reached. It is advisable to wait for during at least half an hour to guarantee that the value of moisture is stable.

2 Then the tip is approached to the surface of the sample at a free amplitude in the range of 4-10 nm (figure 2.2a). Generally, the oxidation is performed in the attractive regime to avoid the contact between the tip and the sample to the extent possible. The free amplitude is calibrated from the optical sensitivity of the cantilever, taking dynamic force curves. With the cantilevers used for the experiments in this thesis, NCH-W (NanoWorld) with an average nominal k of about 40 N/m and f_0 of about 300 kHz, the sensitivity is found to be in the range of 35-40 nm/V.

3 Then, the feedback is switched off and the pulse is applied between the tip and the sample, the sample biased positively with respect to the tip, to form the meniscus (figure 2.2b). The voltages used to form the meniscus and to oxidize are the same in this work. The oxidations are performed with a home built lithographic program, written with a special version of C programming language. It consists in several libraries where groups of specific lithographic functions are defined, such as the application of a pulse with determined amplitude and duration, the translation of the tip in the different axis or the option to describe the coordinates in different coordinate systems (cartesian, polar, cylindrical). It also includes hysteresis and creep correction commands, taking into account the non-linearity effects of the piezoelectric system during the fabrication process.

4 When the oxidation is finished, the feedback is switched on again and the tip retracts from the surface (figure 2.2d).

Figure 2.2e shows how the oxidation process can be monitored by the oscilloscope [71, 74]:

- Label I corresponds to the situation represented in figure 2.2a. Before applying the pulse, the cantilever oscillates at certain amplitude over the silicon surface.

- Label II corresponds to the situation represented in figure 2.2b. Due to the electrostastic forces and the formation of the water meniscus, the oscillation amplitude decreases when the voltage is applied between the tip and the sample and keeps reduced during the fabrication of the oxides.

- Label III corresponds to the situation represented in figure 2.2c. The oscillation amplitude remains damped for a while due to the capillary forces that the water meniscus exerts on the tip after the end of the pulse.

- Label IV corresponds to the situation represented in figure 2.2d, when the feedback is on again, the water meniscus stretches until is broken and the oscillation recovers its original amplitude.

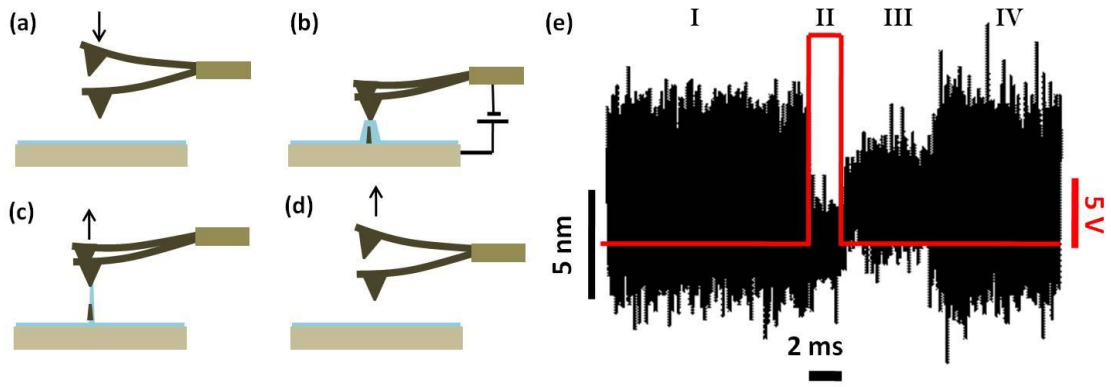

Figure 2.2. Scheme of the oxidation process. (a) The tip is approached to the surface few nanometers of distance. (b) The feedback is switched off and a voltage pulse is applied between the tip and the sample, the sample biased positively with respect to the tip. A water meniscus is formed and the oxidation process takes place. (c) The oscillation amplitude remains damped for a while due to the capillary forces that the water meniscus exerts on the tip after the end of the pulse. (d) The feedback is switched on again, the water meniscus has broken and the oscillation recovers its original amplitude. (e) The oxidation process can be monitored in real time by the output signal of the cantilever deflection registered with an oscilloscope. Labels I, II, III and IV corresponds to, respectively, the situations represented in (a), (b), (c) and (d).

A resistance in the order of MΩ is connected between the holder and the pulse generator in serial to limit the current that flows between the tip and the sample (figure 2.3).

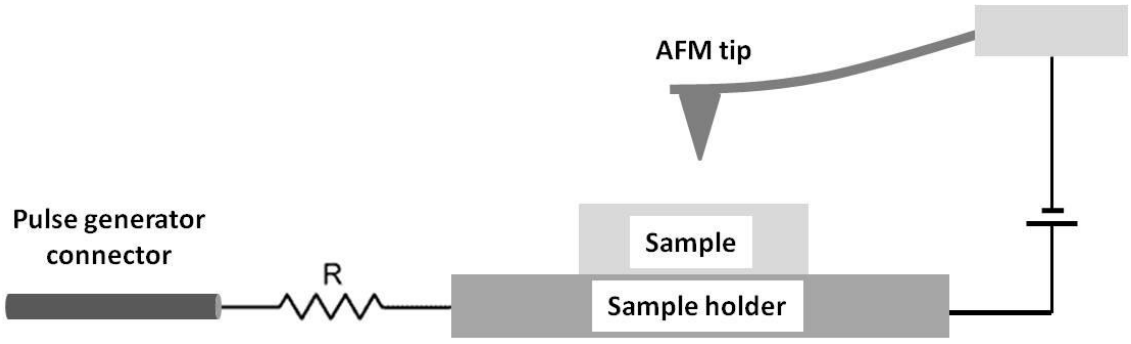

Figure 2.3. A resistance in the order of MΩ has to be connected between the holder and the pulse generator to limit the current that flows between the tip and the sample when a bias voltage is applied between them.

This measure is adopted in order to avoid the apparition of volcano-shaped structures like the ones represented in figure 2.4. This type of structures or similar ones have been reported previously by Xie *et al* [149, 150]. The authors attribute the origin of these structures from stochastic electroshock waves depending on the oxidation conditions. The parameters of oxidation for the array of dots represented in fig 2.4a are: 58.5% of relative humidity, 21 V, 25 μs, and 8 nm of free amplitude. It can be observed that the fabrication of the volcano-like structures is random. Figure 2.4b shows two patterns that have been fabricated at the same time at 51.3%, 18 V, 25 μs and 5.5 nm of free amplitude. However, one of them is a regular oxide with 30 nm of width and 2 nm high (right pattern), while the other is a volcano-like structure (left pattern) with a core diameter about 60 nm and a depth of 1 nm with respect to the surface (figure 2.4d).

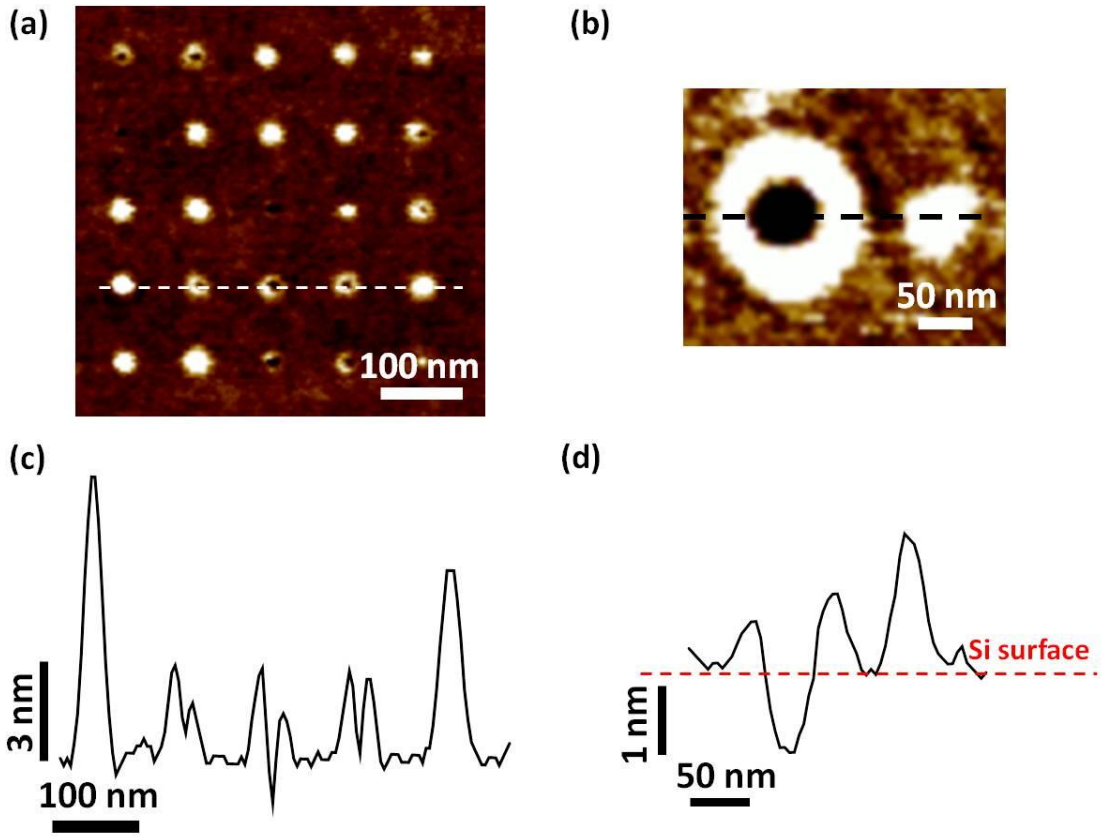

Figure 2.4. (a) AFM image of an array of 5x5 dots with oxides and volcano-like structures. (b) AFM image of another volcano-like structure located next to a normal oxide. (c) AFM cross section of the row marked in white line from (a). (d) AFM cross section of the row marked in black line from (b). The dashed red line corresponds to the baseline of the silicon surface.

2.3 Geometry of the oxide patterns fabricated by oxidation scanning probe lithography

The vertical growth of the oxide happens above and below the silicon surface. To measure the depth of the oxide under the surface, an array of silicon oxide lines has been fabricated, represented in figure 2.5a. Then, these stripes have been etched away by exposing them to HF 10% vapor during 10 s. Finally, the depth of the grooves left after the removal of the oxides, represented in figure 2.5b, has been measured.

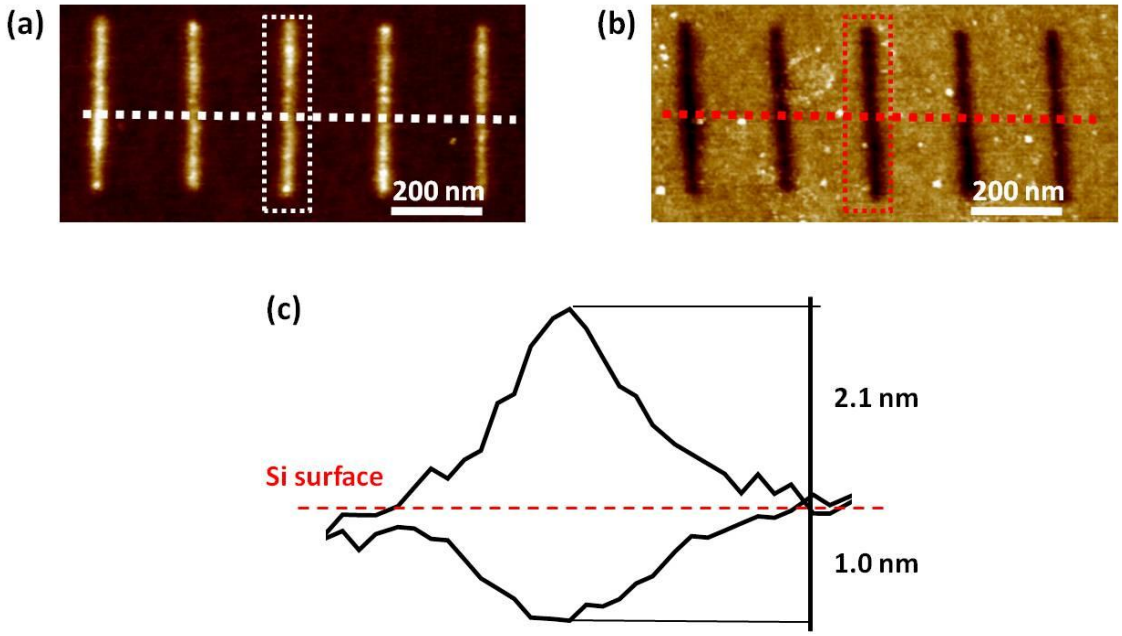

Figure 2.5. (a) AFM image of an array of oxide lines. (b) AFM image of the grooves left after the removal of oxide lines shown in (a) by HF etching during 10 s. (c) AFM cross sections of the oxide (marked by the white dashed rectangle in (a)) and its groove (marked by the red dashed rectangle in (b)), from the dashed lines underlined in (a) and (b). The red dashed line in (c) refers to the baseline of the silicon surface.

The average values of height (h) and depth (d) of the oxides and grooves arrays from figure 2.5 are given in table 2.1. The growth below the surface represents about 35% of the total vertical growth. The h/d ratio value is between 1.7-1.9, and the expansion volume value, (h+d)/d, is about 2.9. These results are very similar to other previous works on silicon (100)-oriented *p*-type [1, 94].

Height (nm)	Depth (nm)	Total thickness (h+d) (nm)	% below surface	Expansion volume (h+d/d)
2.3	1.2	3.5	34.7	2.9

Table 2.1. Average values of the height, depth, percentage of oxide grown below the surface and expansion volume of the features from the array represented in figure 2.5.

The oxides obtained by o-SPL have a trapezoidal shape and the angle of their walls with respect to the horizontal plane is in the range of 1º - 7º (figure 2.6).

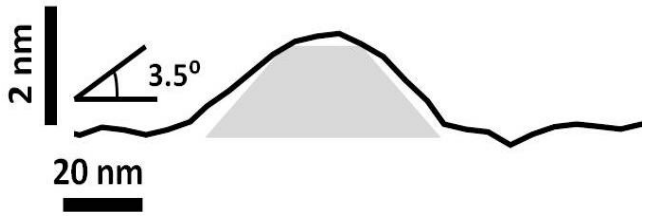

Figure 2.6. AFM cross section of a typical oxide fabricated by o-SPL. The oxidation parameters are 15 V, 1 ms, 40% of relative humidity and 5 nm of free amplitude. The shape of the pattern is close to trapezoidal.

The main application of the o-SPL features in this thesis is their use as etching masks for pattern transfer. For this reason, each time a new AFM tip is used to oxidize, the parameters of oxidation, mainly voltage pulse amplitude, oxidation time and relative humidity, are optimized to have oxide patterns with the smallest width and the maximum angle possible. An example of this calibration of oxidation parameters is represented in figure 2.7. Two series of dots are represented in figure 2.7a and figure 2.7b, fabricated at 40% of relative humidity, 5 nm of free amplitude and oxidation times of 0.5, 1, 10, 100 and 1000 ms (from left to right), with the same tip. The only difference is the applied voltages; 15 V in the case of 2.7a and 21 V in the case of 2.7b. From the graphics of the width (figure 2.7e) and height (figure 2.7f) as a function of the oxidation time for both series it can be observed that the difference in the widths is more pronounced than in the heights for the two voltages. In the case of the dots fabricated with an oxidation time of 1 s (figure 2.7g), both have almost the same height, but the width of the oxide fabricated at 15 V is about 50 nm, while the width of the oxide fabricated at 21 V is about 80 nm. The angle of the oxide with respect to the horizontal plane fabricated at 15 V and 21 V are 5.9º and 3.1º, respectively. Then, with the rest of the parameters fixed, the oxide fabricated at 15 V is a better etching mask than the one fabricated at 21 V because for the same height, it gives a smaller width and a steeper slope.

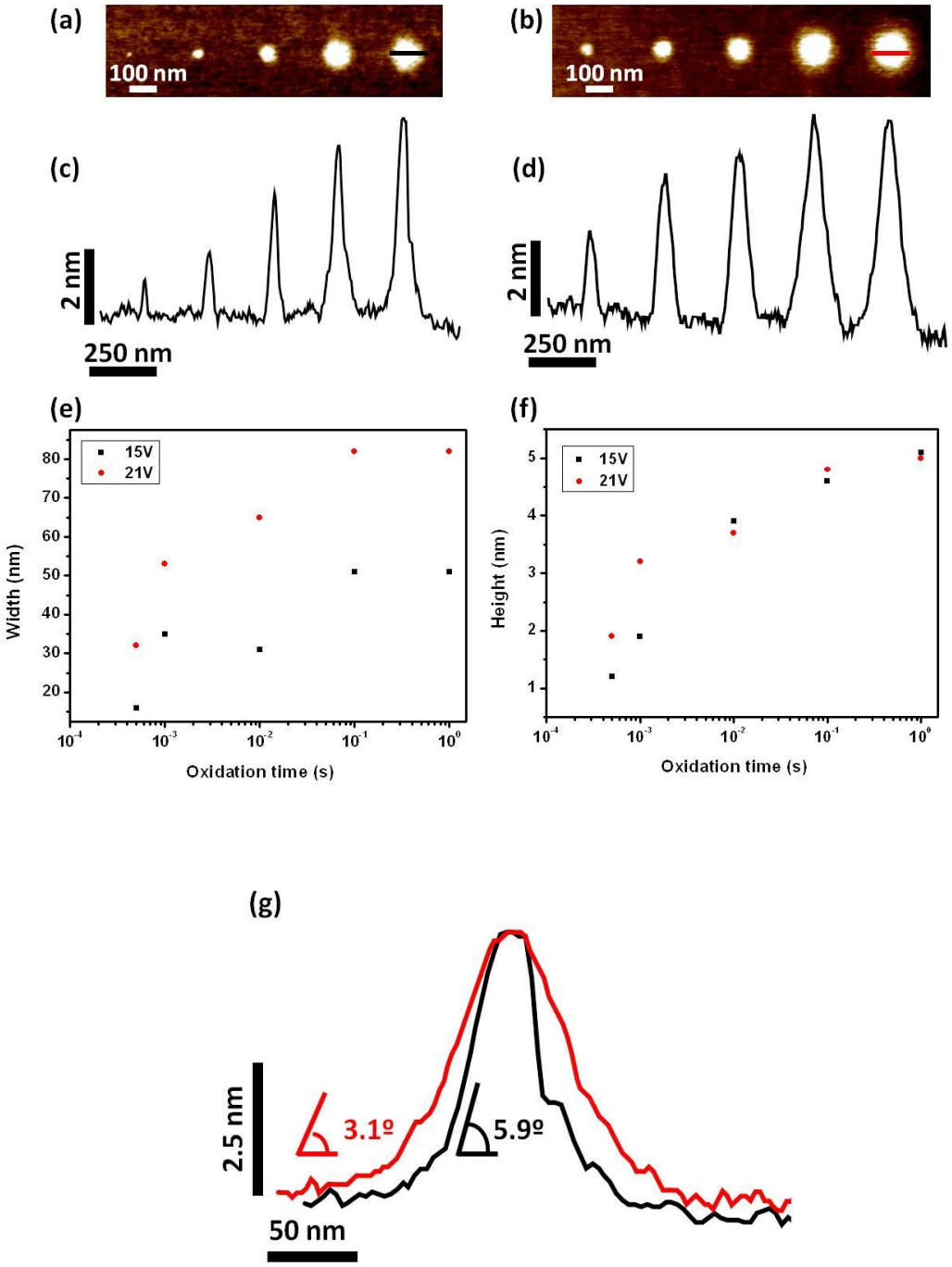

Figure 2.7. (a) AFM image of a series of dots fabricated at 15 V and 0.5, 1, 10, 100 and 1000 ms (from left to right). (b) AFM image of a series of dots fabricated at 21 V and 0.5, 1, 10, 100 and 1000 ms (from left to right). (c) AFM cross section of the patterns represented in (a). (d) AFM cross section of the patterns represented in (b). (e) Width of the dots given in (a) and (b) as a function of the oxidation time. (f) Height of the dots given in (a) and (b) as a function of the oxidation time. (g) AFM cross sections and angles with respect to the horizontal plane of the oxides remarked in (a) (black) and (b) (red). The series of dots in (a) and (b) have been fabricated with the same relative humidity at 40% and free amplitude of 5 nm, using the same tip.

2.4 Optimal conditions for the fabrication of etching masks by oxidation scanning probe lithography

The main application of oxidation scanning probe lithography in this thesis has been the fabrication of oxide lines to use them as etching masks for the fabrication of silicon nanowires. Then, the oxidation parameters and the AFM tip have to be chosen to achieve good resolution and reproducibility.

When the AFM tip has more than one apex or has attached particles in its end, an array of repetitive patterns can be observed such the one shown in figure 2.8a. This means either that each protrusion forms a meniscus and creates multiple patterns or that the visualization of multiple patterns is due to a tip artifact during the imaging step. In any case, this kind of tips has to be discarded to perform o-SPL.

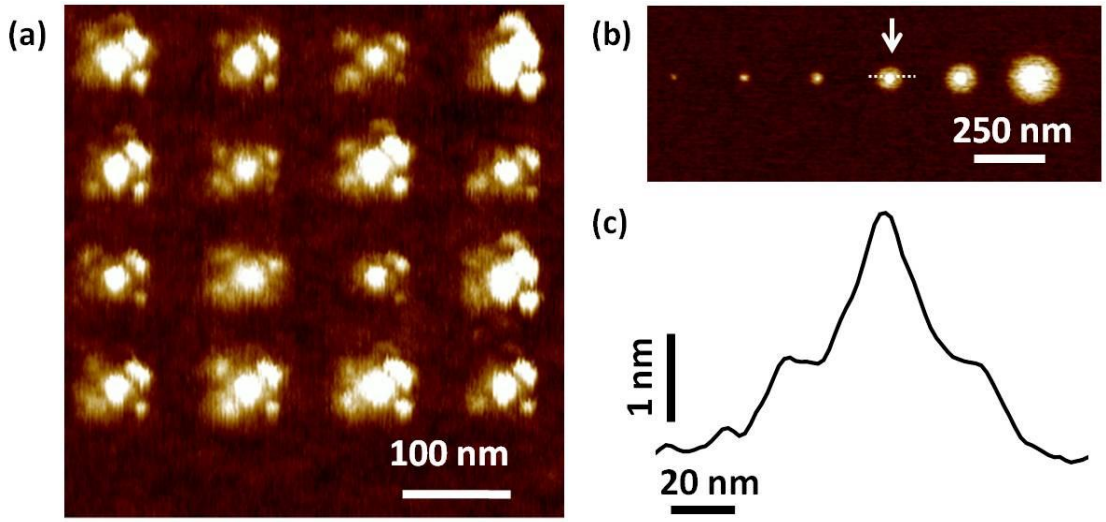

Figure 2.8 (a) AFM image of an array of oxide dots taken with a tip that ends with more than one apex. The visualization of multiple patterns instead of a single dot could be due to a tip artifact or they could be real structures produced by the oxidation of several protrusions. (b) AFM image of an array of dots with two regions of oxidation. (c) AFM cross section of the pattern pointed out in (b). The dot was fabricated at 24 V, 50 ms, 60% of relative humidity and 8 nm of free amplitude.

Under certain conditions, normally at high relative humidity (≥ 60%) and long oxidation times (≥ 10 ms), oxides which have shapes with two different regions are produced (figure 2.8c). These patterns have a sharper profile just in the region below the tip and a wider halo towards the edges of the meniscus. This is probably due to the lateral diffusion of the anions for the high relative humidity and oxidation time. This kind of feature is not suitable as etching mask because it is inhomogeneous and wide.

Once the oxidation parameters are optimized for a given tip, the pattern size reproducibility can extend over thousands of oxides. For example, figure 2.9a shows an array of 6000 points with 50 nm of periodicity which has been fabricated by applying 27V, 1 ms, 45% of relative humidity and about 5 nm of free amplitude. The width of the dots is in the range of 15 nm - 20 nm. The throughput of thousands of oxides is low because of the tip lifetime. With the use, the tip requires higher voltages to oxidize or stops oxidizing. It is probable that the silicon tip ends being oxidized, so it becomes less conductive.

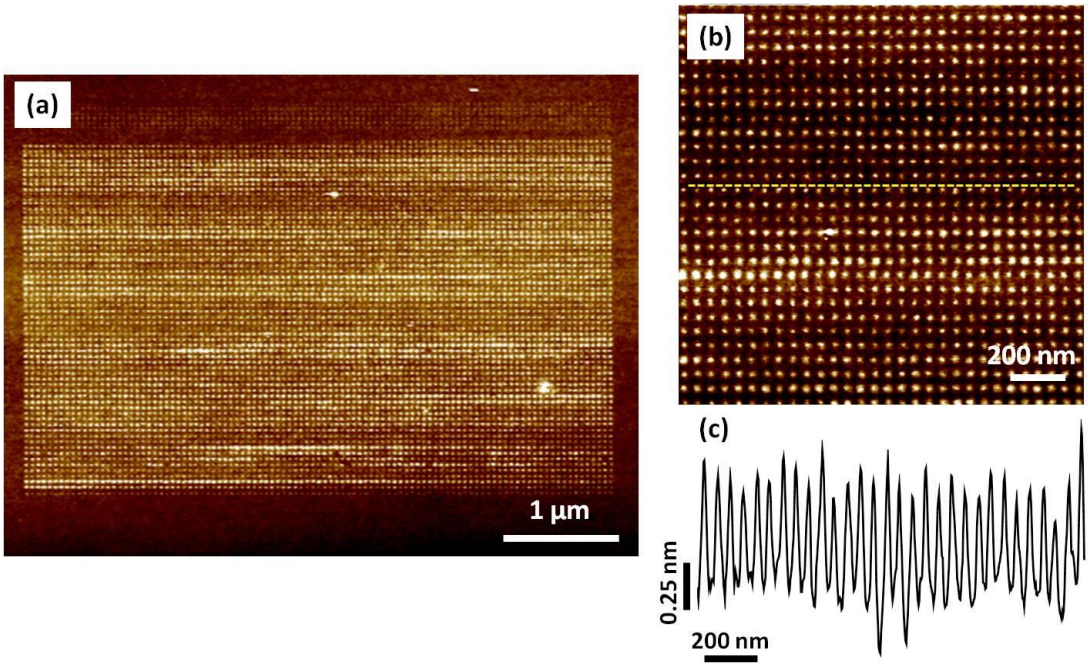

Figure 2.9 (a) AFM image of an array of 60x100 dots fabricated by applying a voltage pulse of 27 V and 1 ms, at 45% of relative humidity and 5 nm of free amplitude. (b) AFM image of the region zoomed from the array in (a). (c) AFM cross section of the array across the line marked in (b).

For similar oxidation parameters (pulse voltage, oxidation time, relative humidity and free amplitude), the resolution of the oxide features depends significantly on the AFM tip. For example, the patterns of figure 2.10, figure 2.11 and figure 2.12 have been fabricated using different tips of the same type of cantilever, NCH-W (NanoWorld). The oxide lines from figure 2.10 have been fabricated by applying pulses of 21V and 7 ms, at 45% of relative humidity and about 5 nm of free amplitude. The width of the lines is in the range of 30 nm - 40 nm. The crossed structures shown in figure 2.11 have been fabricated by applying 27V, 3 ms, 44% and 5 nm of free amplitude. The width of the lines is in the range of 20 - 25 nm. The array of lines with 15 nm periodicity represented in figure 2.12 was fabricated by applying pulses of 24 V and 0.5 ms, at 43% of relative humidity and about 5 nm of free amplitude. These oxidation parameters are very close to the ones used to make the patterns shown in figures 2.10 and 2.11. However, in this case, the features have an average width of 7.5 nm, a factor of 4 smaller than the smallest lines in figure 2.10.

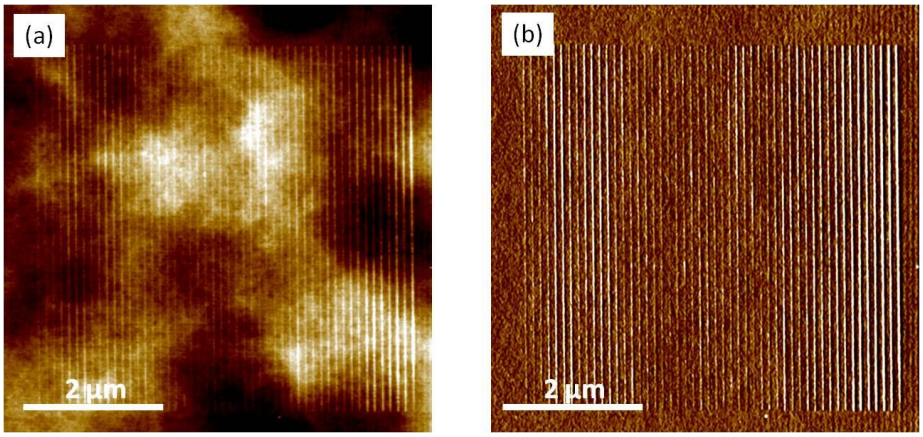

Figure 2.10. AFM topographic (a) and phase (b) image of an array of 50 lines fabricated by applying 21 V, 7 ms, 45% of relative humidity and 5 nm of free amplitude. The periodicity of the lines is 100 nm. The whole fabrication process took 30 minutes.

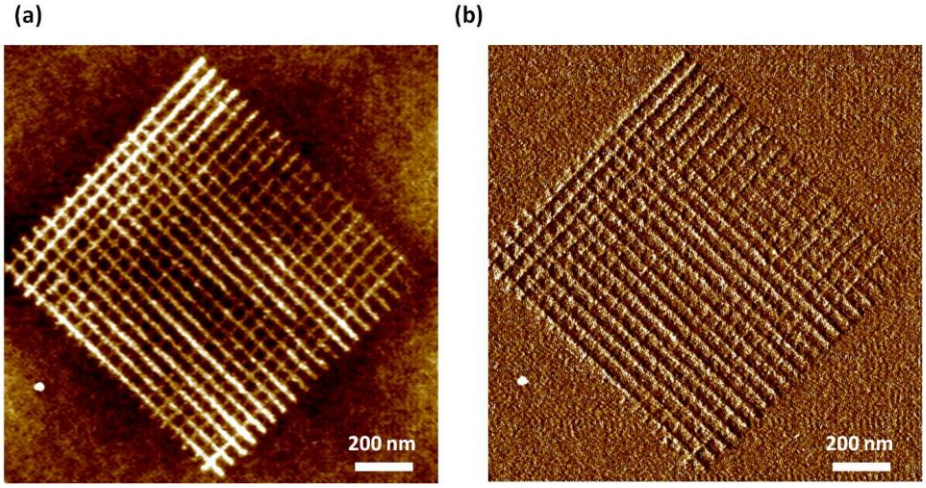

Figure 2.11. AFM topographic (a) and phase (b) image of a crossed structure consisting in 20 lines over 20 lines rotated 90º, fabricated by applying 27 V and 3 ms, at 44% of relative humidity and 5 nm of free amplitude.

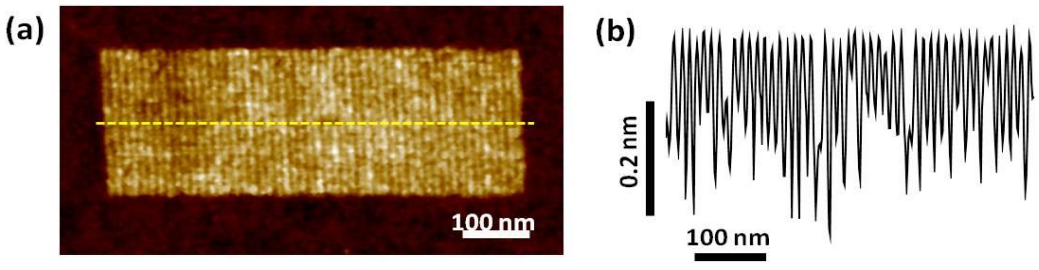

Figure 2.12. (a) AFM topographic image of an array of 50 lines with 15 nm of periodicity, fabricated by applying 24 V, 0.5 ms, 43% of relative humidity and 5 nm of free amplitude. (b) AFM cross section of the array across the line marked in (a).

2.5 Chapter summary

The main points of this chapter are:

- The formation of the water meniscus under an applied voltage pulse and the oxidation process can be monitored with an oscilloscope by having access to the output signal of the cantilever deflection.

- The patterns fabricated by o-SPL grow also below the surface in the vertical direction.

- The patterns fabricated by o-SPL have a trapezoidal geometry and angles with respect to the horizontal plane between 1º - 7º.

- It is necessary to calibrate the oxidation parameters for each AFM tip in order to obtain the patterns with the best height/width ratio.

- An array of 50 lines with 15 nm of periodicity and 7.5 nm of width has been fabricated by applying a voltage pulse of 24 V and 0.5 ms, at 43% of relative humidity and 5 nm of free amplitude.

Chapter 3

Oxidation scanning probe lithography as a top-down approach to make SiNW FETs: Fabrication steps and electrical properties

Silicon is the key material in the microelectronics manufacturing. It keeps on being relevant as one-dimensional material, specifically as a nanowire, for several reasons:

- There are available a large variety of methods to synthesize/ fabricate silicon nanowires (SiNWs), single or in large arrays, with planar configuration or as nanopillars. Most of the top-down fabrications rely on the transfer of patterns into silicon on insulator (SOI) by etching. Some of these approaches are the electron beam lithography [151-153], the catalytic etching [154], the superlattice nanowire pattern transfer (SNAP) [155] or nano imprint lithography (NIL) [156]. On the other hand, vapor-solid-liquid (VLS) mechanism [157, 158], laser assisted catalytic growth [159], low pressure chemical vapor deposition (LPCVD) [160, 161] or solution-grown in supercritical fluid environment [162] are among the bottom up synthesis. Usually, both top-down and bottom-up methods are combined with a thermal oxidation step to further decrease the diameter of the nanowire [163].

- Due to their decrease in the size and their high surface/volume ratio, silicon nanowires present new or improved properties with respect to the bulk such as giant piezoresistivity [164, 165] or enhanced thermoelectricity [166].

- Silicon nanowires can be exploited in a wide range of applications including photonics/solar cells [167, 168], free-label biosensors [169, 170], explosive detectors [171], energy conversion [172] or nanoelectromechanical (NEMS) resonators [173-175].

- Silicon-based field effect transistors in the nanowire configuration allow tailoring the electrical properties, for example, by making heterostructures like core-shell SiGe NWs [176].

Up to now, several works have demonstrated the fabrication of silicon nanowire field effect transistors (SiNW FETs) by o-SPL [135, 136, 138-141] and the use of these devices as a label-free biosensor for molecular recognition [5]. However, the regular use of the o-SPL devices as sensors is limited by the reproducibility of the electrical properties and the low throughput. A good throughput of devices working with a stable conduction response requires the optimization of the fabrication protocol for any type of lithography approach, not only for o-SPL [177]. One way to address this issue is a good characterization of the device electrical properties.

In this chapter, the fabrication of SiNW FETs by o-SPL and the characterization of their electrical properties will be described.

In order to have a quantitative estimation of the quality of the electrical properties of the o-SPL fabricated SiNW FETs with respect to other methods, similar devices have been fabricated by electron beam lithography (EBL) and their transistor characteristics, subthreshold swing (SS) and mobility, have been compared. The comparison of these figures of merit of a transistor is also extended to values from similar devices fabricated by other methods found in the literature, both top-down and bottom-up.

The SOI substrates used in this chapter have a 57 nm thick Si top layer with a nominal resistivity of ρ=10-20 Ω•cm and a 151 nm thick oxide layer, SIMOX (Separation by Implantation of Oxygen) (IBIS Technology, Danvers, MA).

The description of the electrical properties of the devices given in this chapter comes from the study of a sampling which comprises 5 o-SPL and 6 EBL working transistors.

3.1 Oxidation scanning probe lithography fabrication process.

The steps of the SiNW FET fabrication process by o-SPL are:

1. Cutting and cleaning of SOI substrates. The SOI was cleaned by sonication using a protocol of three cycles in NH_4OH:H_2O_2:H_2O (1:1:2) for 12 min each and a last cycle of 5 min in deionized (DI) water. A fresh NH_4OH:H_2O_2:H_2O bath was used in each cycle.

2. Photolithography to define metal electrodes to localize the oxide masks. Experimental conditions:
    - Spin coating of the photoresist S1813 at 3500 rpm for 30s
    - Curing step: baking in 90°C furnace for 30 minutes or in hot plate at 115°C for 60 s
    - Exposure to UV light for 35s with an aligner.
    - Developing step in MF-319 solution for 60 s.

3. Deposition of 5 nm of Cr and 40 nm of Au with the electron beam evaporator (FENIX).

4. Lift-off into acetone for 1 minute under sonication.

5. Fabrication of SiO_2 masks between the marker electrodes by o-SPL in amplitude modulation mode. Typical values of the parameters used to write the oxide lines are applied pulses of 15-30 V, oxidation times in the order of ms and a relative humidity of 40% - 60%. The produced silicon dioxide masks under these conditions have heights between 2-4 nm.

6. Photolithography to define the metal/nanowire contacts. In this step, the SiO_2 masks are contacted with the first marker electrodes. All the experimental conditions are the same as the ones described in step 2.

7. Deposition of 5 nm of Cr and 40 nm of Au with the electron beam evaporator (FENIX).

8. Transfer of the pattern of the oxide mask to the silicon layer of the SOI by reactive ion etching (RIE) (PlasmaLab 80, Oxford Instruments). The etching conditions are a gas mixture of SF_6:O_2 (12:3) sccm, 150 W of rf-power, 90 mTorr of chamber pressure and an etching time between 8-12 s.

After the last step, the final configuration of the device is obtained: a back-gated field-effect transistor, where the nanowire between the source and drain metal electrodes acts as the transistor channel, the SiO_2 layer below acts as the gate dielectric and the silicon substrate is used as the back gate.

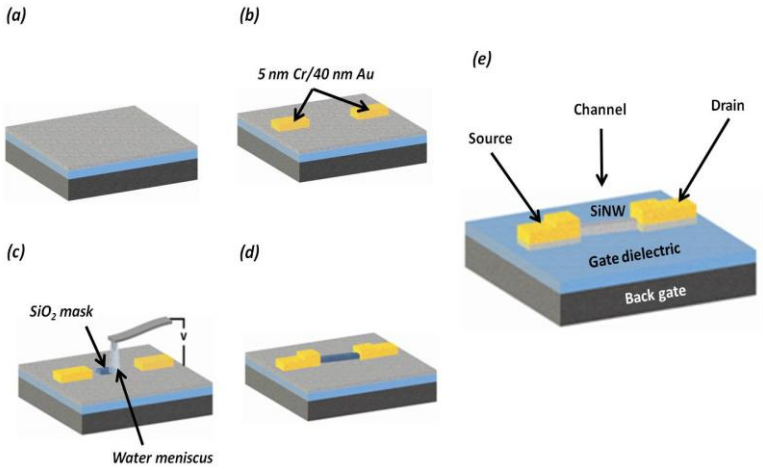

Figure 3.1. Scheme of the fabrication process of SiNW FETs by o-SPL. (a) SOI substrate cutting and cleaning. (b) First metal contacts by photolithography. (c) Oxide mask fabrication by o-SPL. (d) Contacting the oxide mask with the metal electrodes by photolithography. (e) RIE and final configuration of the device.

3.2 Electron beam lithography fabrication process.

The main elements of the electron beam lithography (EBL) system used to make the devices in this thesis (figure 2.2) are:

- A scanning electron microscope (SEM), LEO 145 (LEICA), with LaB_6 filament and 25 KeV of beam energy. This SEM has a sample plate equipped with a laser interferometer stage with stitching capabilities of 2.500 writing fields (tipical size of 100 x 100 μm^2).

- A 2 MHz pattern generator, the Elphy-Plus (Raith, gmbH) incorporated with a software which allows the calculation and adjustment of the exposure parameters and the alignment with previous structures.

- A GDSII layout editor/viewer

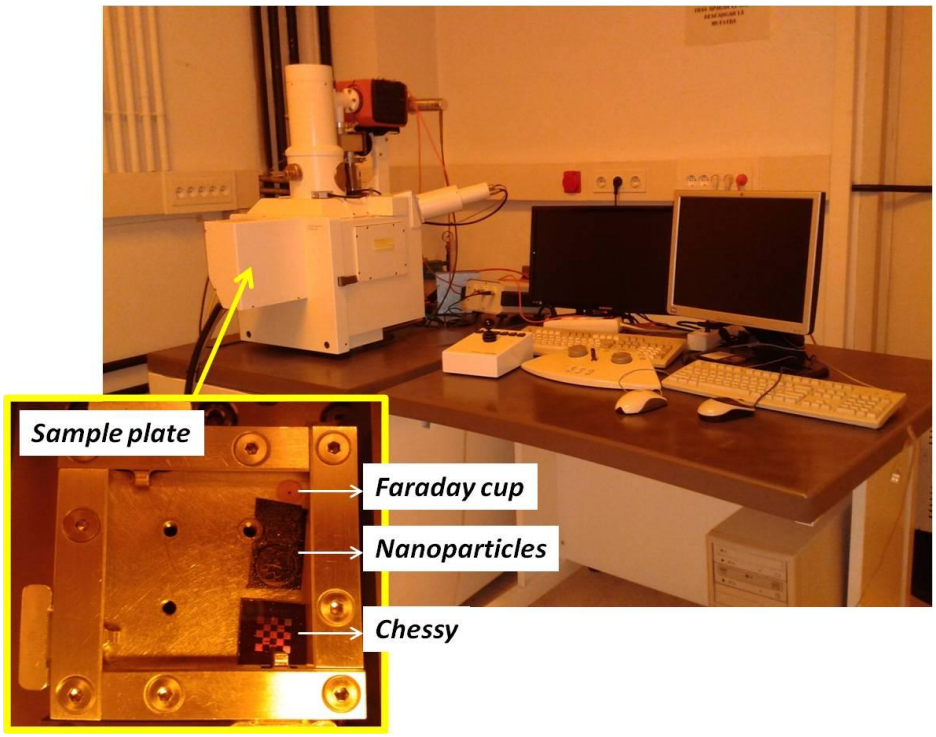

Figure 3.2. EBL system used to fabricate the SiNW FETs. Inset: sample plate with a Faraday cup to adjust the beam current intensity, gold nanoparticles to correct the astigmatism and a chessy calibration standard to focus.

The steps of the SiNW FET fabrication process by EBL are:

1. Cutting and cleaning of SOI substrates. The SOI was cleaned by sonication using a protocol of three cycles in $NH_4OH:H_2O_2:H_2O$ (1:1:2) for 12 min each and a last cycle of 5 min in deionized (DI) water. A fresh $NH_4OH:H_2O_2:H_2O$ bath was used in each cycle.

2. Photolithography to define the metallic contacts.
   Experimental conditions:
   - Spin coating of the photoresist S1813 at 3500 rpm for 30s
   - Curing step: baking in 90ºC furnace for 30 minutes or in hot plate at 115ºC for 60 s
   - Exposure to UV light for 35s with an aligner.
   - Developing step in MF-319 solution for 60 s.

3. Deposition of 5 nm of Cr and 40 nm of Au with the electron beam evaporator (FENIX).

4. Lift-off step into acetone for 1 minute under sonication.

5. Spin coating of the negative tone resist AR-N 7500.08 (Allresist GmbH, Strausberg, Germany) at 4000 rpm during 60 s. Curing at 85ºC during 60 s.

6. Definition of the resist line masks between the metal contacts by EBL. Typical values of exposure are: an intensity current of about 50 pA and a line dose in the range of 4000-6000 $\mu A \cdot s/cm^2$.

7. Developing step with the mixture of (4:1) AR 300-47 (Allresist GmbH, Strausberg, Germany): DI H_2O during 80 s to remove the unexposed areas of the resist.

8. RIE to transfer the pattern of the oxide mask to the silicon layer of the SOI. The RIE system used in this thesis is a PlasmaLab 80 (Oxford Instruments, UK). The etching conditions are a gas mixture of $SF_6:O_2$ (12:3) sccm, 150 W of rf-power, 90 mTorr of chamber pressure and etching time between 8-12 s.

After the last step, the final configuration of the device is obtained, which is very similar to the one fabricated by o-SPL process: a back-gated field-effect transistor, where the nanowire between the source and drain metal electrodes acts as the transistor channel, the SiO_2 layer below acts as the gate dielectric and the silicon substrate is used as the back gate.

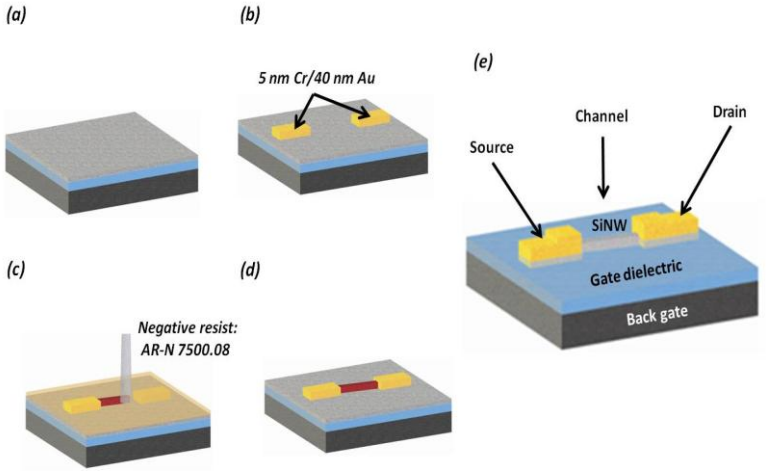

Figure 3.3. Scheme of the fabrication process of SiNW FETs by EBL. (a) SOI substrate cutting and cleaning. (b) Metal contacts by photolithography. (c) Resist mask line definition by EBL. (d) Developing step to remove the unexposed areas. (e) RIE and final configuration of the device.

3.3 Main characteristics of a field-effect transistor

There are two main ways to represent the I - V curves of a transistor [178]:

- The output characteristics represent the source-drain current (I_{ds}) as a function of the source-drain voltage (V_{ds}) for different gate voltages (V_g). The output curves give information about the type of device according to the channel carriers and according to the current level at zero gate bias. If the current level increases with the negative gate bias ($V_g < 0$), the device is a ***p*-channel** field-effect transistor (FET) and the carriers of the channel are holes (figure 3.4a). If the current level increases with the positive gate bias ($V_g > 0$), the device is an ***n*-channel** FET and the carriers of the channel are electrons (figure 3.4b). If the current level is very small at zero voltage bias and a gate voltage has to be applied to turn the FET on, the device is called normally-off or **enhancement-mode** FET. If the current level is different to zero at $V_g = 0$ and a gate voltage has to be applied to turn the FET off, the device is called normally-on or **depletion-mode** FET.

- The transfer characteristics represent the source-drain current (I_{ds}) as a function of the gate voltage (V_g) at a fixed source-drain voltage (V_{ds}). The types of transfer curves according to the type of FET channel are shown in figures 3.4c and 3.4d. This kind of I - V representation is more straightforward to extract some figures of merit of the FETs such as the subthreshold swing (SS), the ON/OFF current ratio and the threshold voltage (V_{th}), which will be explained below.

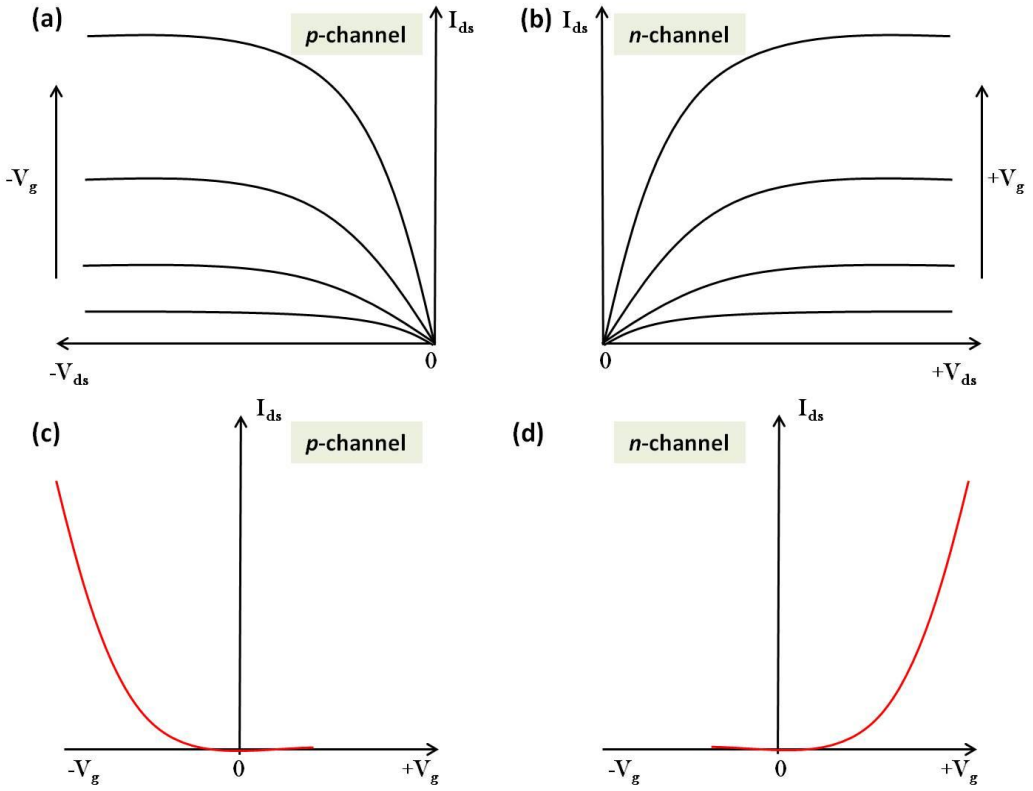

Figure 3.4. (a) Output characteristics of a *p*-channel FET. The current level increases by applying increasing negative gate bias ($V_g < 0$). (b) Output characteristics of an *n*-channel FET. The current level increases by applying increasing positive gate bias ($V_g > 0$). (c) Transfer characteristics of a *p*-channel FET. (d) Transfer characteristics of an *n*-channel FET.

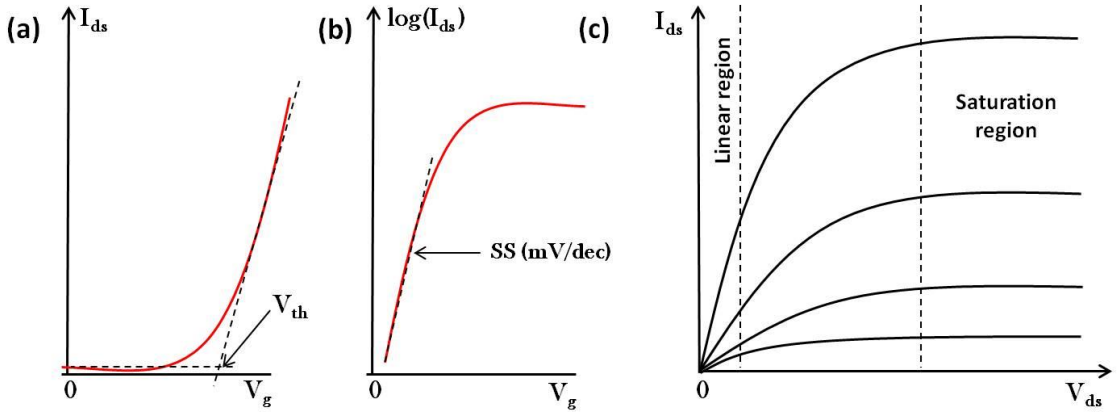

Figure 3.5. (a) The threshold voltage (V_{th}) can be extrapolated from the transfer curve represented on a linear scale. (b) The subthreshold swing (*SS*) can be calculated from the slope of the transfer curve represented on a logarithmic scale in the subthreshold region. (c) Two different regions can be distinguished from the output curves. In the linear region, the source-drain current increases linearly with the source-drain voltage. In the saturation region, the source-drain current has reached a constant value that becomes independent of the source-drain voltage.

The main figures of merit of a FET are the threshold voltage (V_{th}), the ON/OFF current ratio, the subthreshold swing (SS) and the mobility (μ). The first three can be extracted directly from the transfer curves.

- The threshold voltage can be extrapolated from the transfer curve represented on a linear scale as the intersection of the slope with the OFF current level (figure 3.5a).

- The ON/OFF current ratio is estimated from the transfer curve represented on a logarithmic scale (3.5b).

- The subthreshold swing is defined as the change in the gate voltage needed to change the source-drain current in one order of magnitude (mV/dec) and gives information of how fast a transistor turns off or on when a gate voltage is applied. Then, the smaller the SS is, the better the transistor will be. The SS can be estimated experimentally from the slope of the transfer curve represented on a logarithmic scale (3.5b). Its theoretical expression is:

$$SS = (\ln 10)\left(\frac{kT}{q}\right)\left(1+\frac{C_D}{C_{ox}}\right) \qquad (3.1)$$

  Where kT/q is the thermal energy divided by the elementary charge and C_D, the depletion layer capacitance. From equation 3.1, the minimum SS achievable at room temperature (300 K), considering $C_{ox} \rightarrow \infty$, is 60 mV/dec.

The mobility can be extract in three different ways [178, 179]:

- Taking into account the transconductance G_m at a fixed source-drain voltage:

$$\mu = \frac{L^2 G_m}{C_{ox} V_{ds}} \qquad (3.2)$$

- From the output curves in the linear region (figure 3.5c) as:

$$I_{ds} = \frac{\mu C_{ox}}{L^2} \cdot (V_g - V_{th}) \cdot V_{ds} \qquad (3.3)$$

- From the output curves in the saturation region (figure 3.5c) as:

$$I_{ds} = \frac{\mu C_{ox}}{2L^2} \cdot (V_g - V_{th})^2 \qquad (3.4)$$

L is the channel length and C_{ox} is the gate oxide capacitance, which is explained with detail in section 3.6.2.

G_m is the transconductance and is calculated as the fit of the slope of the transfer curve above the threshold voltage. It is defined as:

$$G_m = \frac{dI_{ds}}{dV_g} \qquad (3.5)$$

3.4 Rapid thermal annealing of the SiNW FETs after the fabrication process.

Once the device has been fabricated, its transistor output and transfer curves are measured in the probe station with a semiconductor analyzer. If the curves give a reliable response, that is, similar current level for the same values of source to drain and gate voltages after several measurements and over several days, then the device is ready to be used for specific applications such as biosensing. However, practically all the field-effect transistors, both thin layer-based and nanowire-based FETs need to undergo a rapid thermal annealing (RTA) treatment to optimize their electrical performance. This thermal annealing has two main purposes, to reduce the density of trapped charges and defects originated during the fabrication process and to improve the metal-semiconductor contact.

The annealing of the devices was performed with a Rapid Thermal Processing (RTP) oven (AS-Micro, Annealsys, France), in which the heating of the sample is produced by irradiation from infrared halogen lamps. In this thesis, the RTP oven was used just to improve the transistor performance of the devices. However, it also can be utilized for thermal oxidation, crystallization processes or activation of dopants. It can be used to heat samples up to 1250ºC with a maximum ramp rate of 50ºC/s.

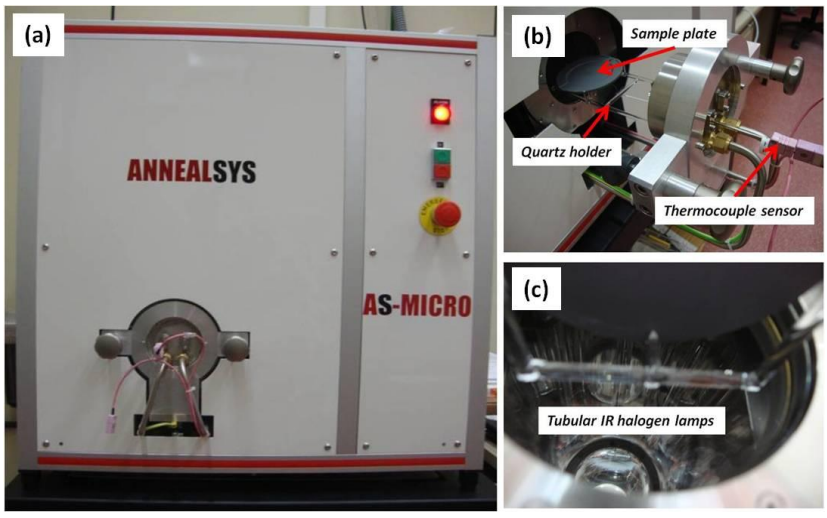

Figure 3.6. (a) Rapid Thermal Processing oven used to anneal the devices. (b) A thermocouple sensor is connected to the sample plate to control the temperature of the process. (c) The heating of the sample is produced by irradiation from infrared halogen lamps.

All the annealing treatments were performed under nitrogen atmosphere. The range of temperatures studied was of 300ºC - 850ºC during 30 s. At 850ºC, most of the devices stopped being conductive. The optimal conditions of RTA treatment for both o-SPL and EBL fabricated transistors were found to be at 300ºC for 30s.

For example, in figure 3.7 there are represented the transfer curves on logarithmic scale of a device fabricated by each method before and after RTA treatment. The source-drain voltage corresponds to 0.5 V. Before the treatment, the subthrehold swing (*SS*) for both type of devices is in the order of 1000 mV/dec. After treatment , the *SS* of both devices improves by a factor of 2. This considerable improvement in the performance of the devices after treatment gives an account of how the several steps involved in the fabrication process affect their electrical properties.

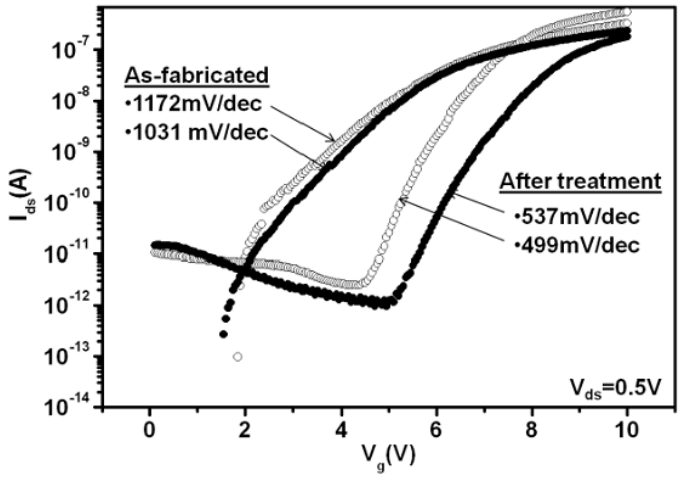

Figure 3.7. Transfer curves of an o-SPL fabricated (open cicles) and an EBL fabricated (filled circles) SiNW FETs before and after the application of a RTA treatment at 300ºC during 30 s in nitrogen.

Another way to estimate the improvement of the device performance introduced by the thermal treatment is to observe the hysteresis of the transistor transfer curve. This hysteresis is taken as the area contained inside the curve when the transfer is measured with forward and reverse sweep and it is related to trapped charges in the silicon oxide or in the surface of the silicon nanowire [180, 181].

In figure 3.8, it is represented the double-swept transfer curve of an o-SPL fabricated SiNW FET before (figure 3.8a) and after (figure 3.8b) a treatment of 300ºC and 30s in nitrogen. The source-drain voltage corresponds to 0.5 V. After the treatment, apart from the fact that the slope of the transfer curve is steeper, which means that the *SS* is smaller, the area enclosed in the curve is smaller. This implies that the treatment has reduced the density of defects.

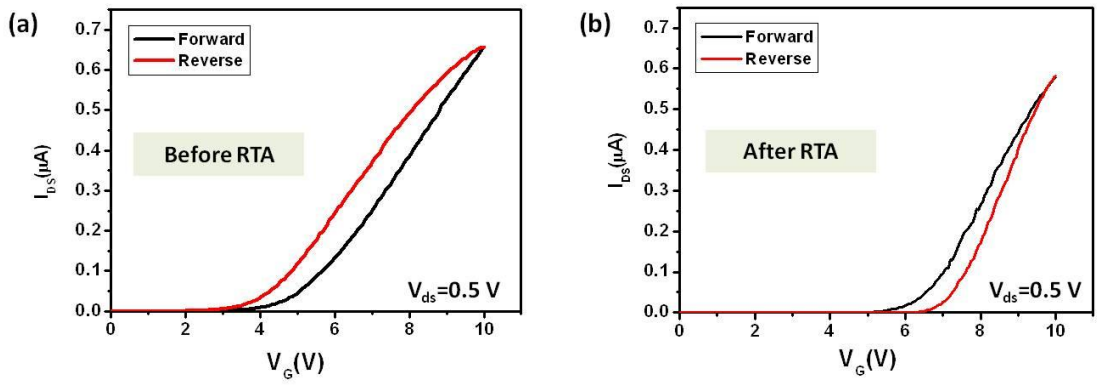

Figure 3.8. Transfer curves of an o-SPL fabricated SiNW FET (a) before and (b) after the application of an RTA treatment at 300ºC during 30 s in nitrogen. After the treatment, the area enclosed in the curve is smaller, which implies that the treatment has reduced the density of defects. Both graphics are represented at the same scale.

The use of higher temperatures for the annealing does not imply that the devices stop working, but their current level decreases and their electrical properties worsen. For example, in figure 3.9 it is represented the double-swept transfer curve of an EBL fabricated SiNW FET before (figure 3.9a) and after (figure 3.9b) a treatment of 400ºC and 30s in nitrogen. The source-drain voltage corresponds to 0.5 V. After the treatment, the hysteresis has been reduced. However, the current level of the nanowire has decreased and the slope of the curve is considerably less steep, which means that the value of the subthreshold swing will be higher than before treatment.

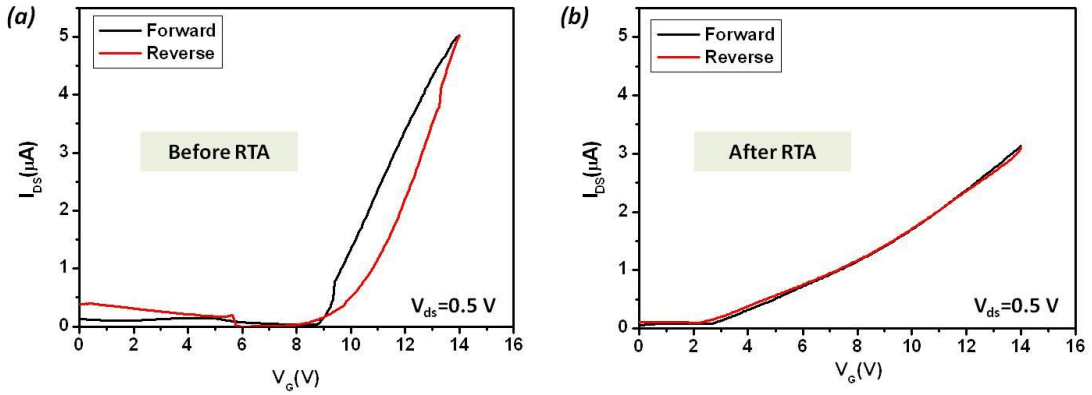

Figure 3.9. Transfer curves of an EBL fabricated SiNW FET (a) before and (b) after the application of an RTA treatment at 400ºC during 30 s in nitrogen. After treatment, the hysteresis has been reduced, but the subthreshold swing has worsened significantly, as the slope of the transfer curve is less steep than before RTA. Both graphics are represented at the same scale.

This can be explained by taking into account the type of metal electrodes used to fabricate these devices: 5 nm of Cr and 40 nm of Au. The treatment at 400ºC during 30 s is enough to induce the change of the contacts, visible both by AFM topography and optical images, shown in figures 3.10b and 3.10h, respectively. The degradation of the metal contacts keeps on increasing for higher temperatures, for instance, at 600ºC (figures 3.10c and 3.10i), and it causes the degradation of the electrical properties. The images in figure 3.10 correspond to the SiNW FET from which the transfer curves given in figure 3.9 were taken.

From the AFM images shown in figures 3.10d, 3.10e and 3.10f, it can be seen that the thermal treatments do not seem to induce structural changes in the silicon nanowire at the vicinity of the metal/nanowire contact, since the AFM images have the same scale in the vertical direction and the observed difference in the widths of the nanowire is due to the fact that the images were taken with different tips each time.

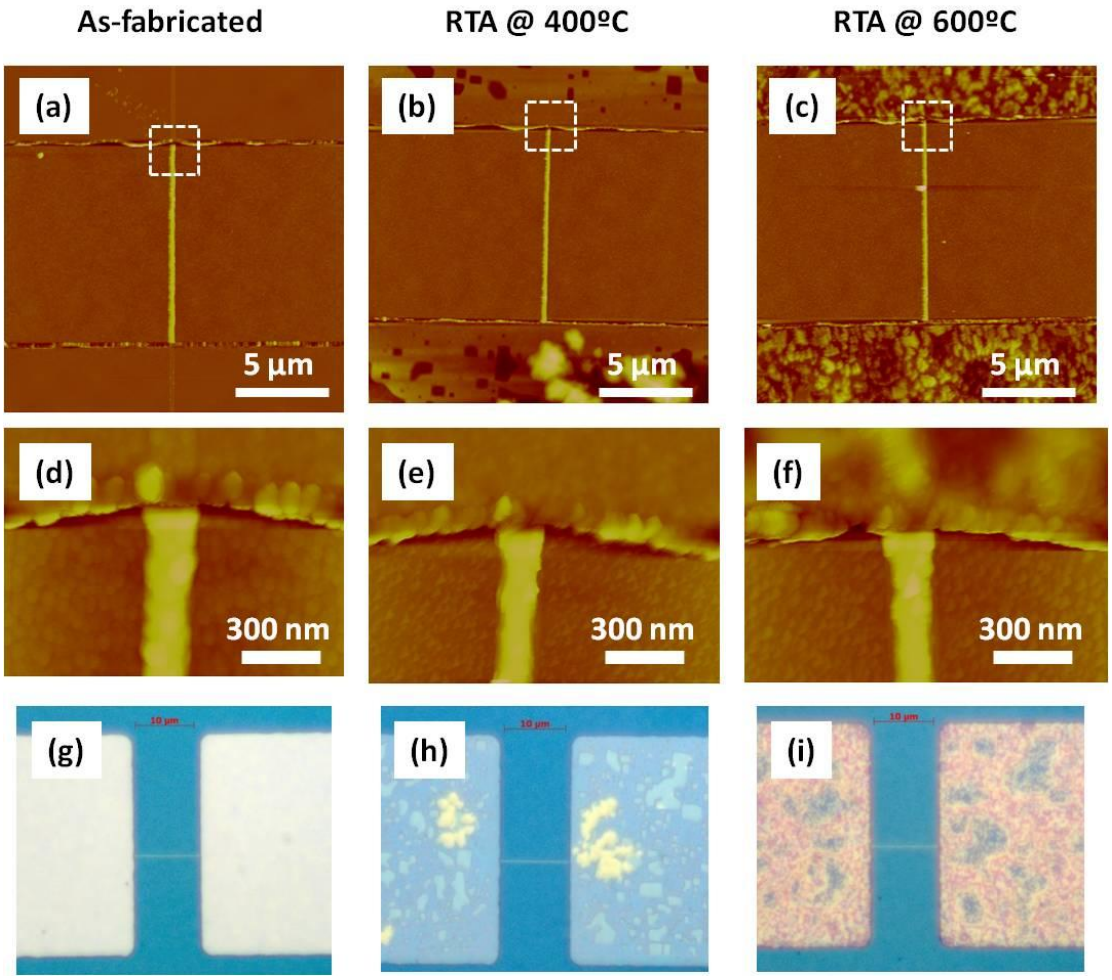

Figure 3.10. AFM topographic images of a SiNW FET (a) As fabricated (b) After an RTA of 400ºC (c) After an RTA of 600ºC. The images are at the same scale. (d), (e), (f) AFM topographic images of the regions marked by the white dashed square in (a), (b) and (c), respectively. The images are at the same scale. (g), (h), (i) Corresponding optical images of (a), (b) and (c), respectively.

To summarize this section, for the metal contacts used to make the devices presented in this chapter, 5 nm Cr/40 nm Au, a thermal rapid annealing treatment at 300ºC for 30 s in nitrogen is found to improve the subthreshold swing of both o-SPL and EBL made transistors by a factor of two without degrading the metallic electrodes.

3.4 Geometry of the devices

The SiNW FETs fabricated by both methods come from the same SOI substrate, which means that the height of the nanowires is mostly determined by the original thickness of the silicon layer of the SOI, in this case, 57 nm. In general, the height of the o-SPL nanowires is smaller, in the order of 30-40 nm, while the height of the EBL nanowires is about 50 nm. This is because the oxide masks defined by o-SPL are much smaller than the resist masks defined by EBL and are entirely consumed during the etching process, given the fact that the same reactive ion etching conditions were used for both cases. The oxide masks have heights between 2 - 4 nm, while the film thickness of the AR-N 7500.08 resist spinned at 4000 rpm for 60 s is about 100 nm.

The fabricated SiNWs were 5-10 μm in length. The nanowire width depends on the lithographic method; the values of width are between 60 to 80 nm in o-SPL case and 100 to 150 nm in the case of EBL.

The SiNWs fabricated by each method differ in their shape. The cross-section of the nanowires fabricated by EBL is close to rectangular, while the cross-section of the nanowires fabricated by o-SPL is trapezoidal. This can be observed from the superimposed AFM cross-sections given in figure 3.11c. The difference in the nanowire shapes is a consequence of the difference in the mask shapes. In the case of o-SPL, the trapezoidal shape of the SiO_2 features is transferred to the silicon nanowire during the etching process, while the EBL method leads to more rectangular wires with quite steep walls.

On one hand, the dispersion in the size of the nanowires fabricated by each method will make their comparison less accurate, since the dependence of the electrical properties on the geometry is clear. However, the observed trend in the output and transfer curves, the current level (I_{ds}) and the transistor characteristics, subthreshold swing and mobility, of all the SiNW FETs analyzed in this chapter are very similar as observed in the rapid thermal annealing section and as will be seen in the next section.

The widths of the SiNWs are given by full width at half maximum (FWHM), unless otherwise indicated.

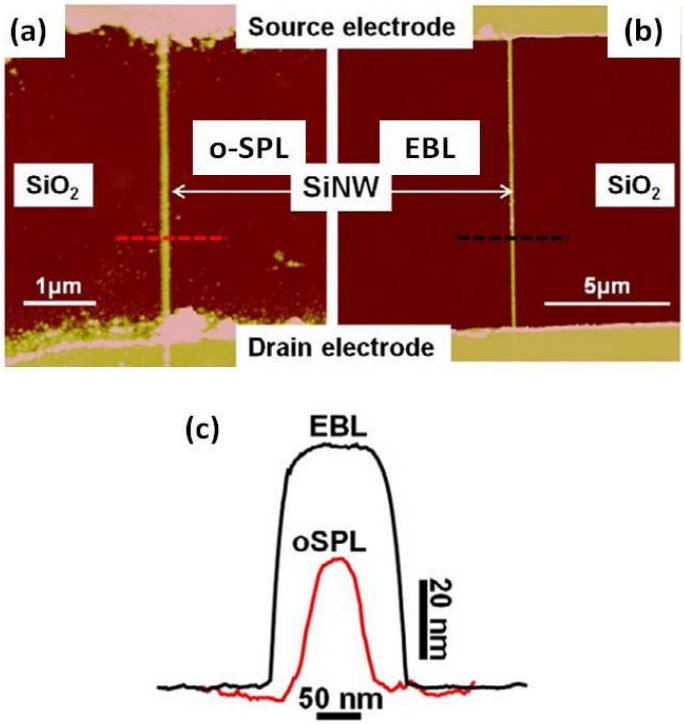

Figure 3.11. (a) AFM image of a SiNW FET fabricated by o-SPL. (b) AFM image of a SiNW FET fabricated by EBL. (c) Superimposed AFM cross sections of the o-SPL device shown in (a) and the EBL device shown in (b).

3.6 Electrical properties of the devices

In this section, the electrical characteristics of the devices fabricated by o-SPL and EBL are addressed: type of transistor, capacitance, mobility, *SS*, and ON/OFF current ratio.

The electrical measurements of the fabricated SiNW FETs were performed at room temperature in a probe station (Everbeing EB 06, Taiwan) with a semiconductor characterization system (Keithley 4200). The instrument is provided with three source/monitor units (SMU), a ground unit (GNDU) and triaxial cables. The measurements consist in recording output and transfer curves from the devices. Two of the tungsten probes are placed in the metallic electrodes to applied source to drain voltages and measure the current which passes through the transistor channel. The third probe is used to modulate the gate voltage of the transistor. The instrument is placed inside a Faraday cage to reduce the noise during the data acquisition. The current sensitivity is in the order of femtoampers.

The set-up of the electrical measurement is represented in figure 3.12.

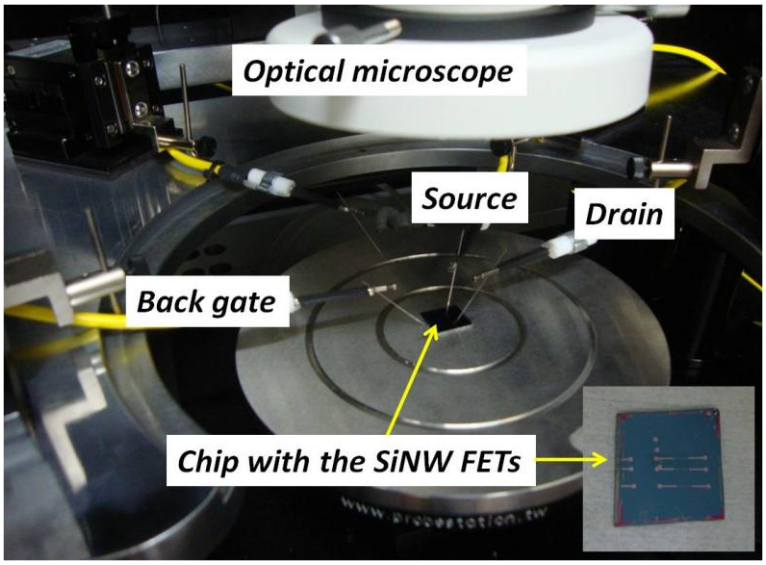

Figure 3.12. Set-up of the probe station with the tungsten probes placed on the chip with the SiNW devices for the measurements of transistor curves. Inset: a chip with three pairs of electrodes with a device in each of them.

All the graphics and results given in this section are from devices optimized by RTA treatment, unless otherwise indicated.

3.6.1. Ambipolarity of the SiNW FETs

Both transistors fabricated by o-SPL and EBL are Schottky barrier field effect transistors (SB-FETs) because their device configuration involves the direct contact between the metal of the electrode and the low doped (10^{-15} cm^{-3}) silicon nanowire channel [182-185]. These types of transistor are attractive because they avoid the use of dopants and parasitic resistances.

The SB-FETs present an ambipolar behavior. This means that the same device can work at the *p*-channel FET regime, which corresponds to the case when the current increases with negative gate voltages and at the *n*-channel FET regime, when the current increases with positive gate voltages (figure 3.13). This is due to the barrier heights for electrons and holes at the metal/SC interface [183, 178]. When a positive gate voltage is applied, the electron barrier height is lowered forming an inversion electron channel. The dominant conduction carriers in this case are the electrons and therefore, the channel will be *n*-type. On the other hand, when a negative gate voltage is applied, the hole barrier height is lowered and an accumulation hole channel is formed. In this case, the channel will be *p*-type.

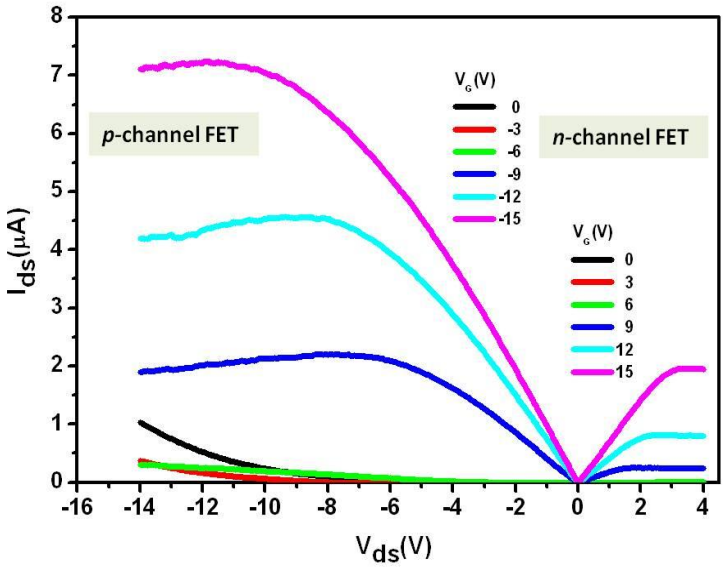

Figure 3.13. Superimposed output curves of the same o-SPL SiNW FET when negative gate voltages (*p*-channel FET) and positive gate voltages (*n*-channel FET) are applied.

Many of the SiNW SB-FETs are ambipolar, with independence of the employed metal contacts, both with or without thermal treatment. Some examples from the literature are represented in table 3.1. The ambipolarity of the FETs can be exploited for logic applications because the same device can work as unipolar *p*-channel or *n*-channel just by choosing the voltage conditions. Moreover, recently, Weber and coworkers have fabricated a device with an axial nanowire heterostructure design to make the SiNW SB-FETs ambipolar on purpose, to use them as electronic devices with programmable behavior [185].

Author (reference)	Metal contacts	Annealing treatment
Koo *et al* [183]	Ti/Au	None
Koo *et al* [183]	Cr/Au	None
Byon *et al* [186]	10 nm NiCr/ 90 nm Au	2 min at 200ºC+5 min 400ºC, vacuum
Colli *et al* [187]	20 nm Ti/ 90 nm Al	30 s at 400ºC, forming gas
Colli *et al* [187]	50 nm Ni	30 s at 400ºC, forming gas
Talin *et al* [188]	Al	20 min at 450ºC, vacuum

Table 3.1. Examples of ambipolar SiNW SB-FETs with their corresponding reference, the metal contacts used and the annealing treatment underwent.

3.6.2 Capacitance of the transistors

The capacitance of the nanowire-dielectric-gate interface (C_{nw}) is needed to calculate the mobility of the transistors.

To estimate the capacitance, two different analytical models and finite-element simulations have been considered for different geometries of the nanowire-oxide-gate interface [179, 189, 190].

The expression for the parallel-plane capacitor model is:

$$C_{nw}^{p} = \frac{\varepsilon_0 \varepsilon_{ox}}{t_{ox}} WL \qquad (3.6)$$

Where W and t_{ox} are respectively, the width of the SiNW channel and the thickness of the dielectric (figure 3.14).

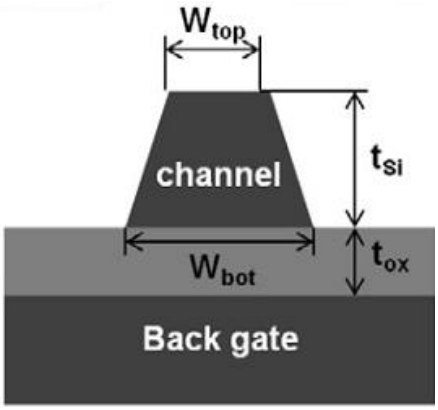

Figure 3.14. Scheme of the cross section of a device with its lateral and vertical dimensions. The EBL-made nanowires are also considered as trapezoidal with $W_{top} \approx W_{bot}$ for simplification.

The expression for the capacitance of a cylindrical nanowire surrounded by a dielectric is:

$$C_{nw}^{C} = \frac{2\pi\varepsilon_0 \varepsilon_{ox}}{\cosh^{-1}(t/R)} L \qquad (3.7)$$

Where t is the distance from the center of the wire to the bottom gate electrode ($t = R + t_{ox}$).

Finally, figure 3.15 shows finite-element simulations (COMSOL Multiphysics) of the electric field lines for the two analytical models described above and for a trapezoidal SiNW (figure 3.14). The latter geometry is very close to that of the fabricated nanowires. The field lines of the cylindrical model are a better approximation to those of the trapezoidal SiNW that those of the parallel-plate model. Thus the cylindrical model is expected to give a better estimation of the capacitance than the planar model. This is verified by calculating the capacitance of a nanowire with a length and height respectively of 10.5 μm and 32 nm. The value of the width is 85 nm and 20 nm for bottom and top

sides (red section in figure 3.11c). For the parallel model the bottom side of the wire is taken. For cylindrical model, the equivalent radius of the trapezoidal nanowire is obtained by matching the area of its section with that of a circle. For the above values we obtain for the parallel, cylindrical and trapezoidal, respectively, 0.2 fF, 0.85 fF and 0.69 fF. Thus, the values of capacitance of the fabricated SiNWs fall between the boundaries defined by the parallel-plate and cylindrical models, and, as expected, the cylindrical model gives a better estimation. The cylindrical model introduces a slight overestimation of the real value because it considers that a uniform dielectric surrounds the SiNW. However, in the fabricated nanowires a dielectric oxide isolates them from the gate electrode but the top and lateral faces of the nanowire are surrounded by air which has a lower relative dielectric constant than the oxide (ε_{air}=1 compared to ε_{ox}=3.9) [190].

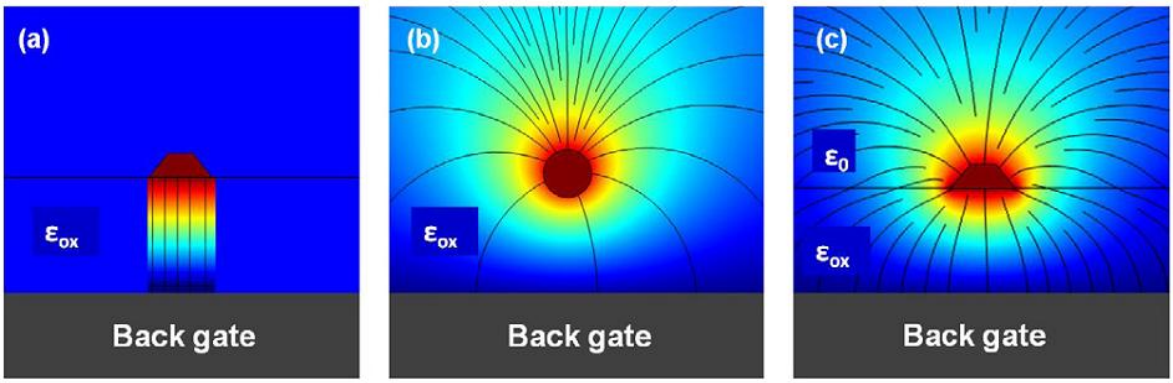

Figure 3.15. Finite-element simulation of the field lines for different models of the nanowire-dielectric-gate interface. (a) Potential drop and electric field lines for a parallel-plate capacitor. (b) Potential drop and electric field lines for a cylindrical model. (c) Potential drop and electric field lines for a trapezoidal Si nanowire on top of a SiO_2 dielectric. The potential drop is illustrated by the color changes.

3.6.3 Mobility and subthreshold swing of the transistors

Once the capacitance has been estimated, the threshold voltage (V_{th}), the subthreshold swing (*SS*), the on/off current ratio and the mobility (μ) will be given. The first three parameters are extracted directly from the transfer curves. The electron mobility is given using equation 3.2.

For the measurement of the mobility and the subthreshold swing, only the *n*-channel of the devices has been considered, since the transistors in inversion mode exhibit saturated conduction for lower source to drain voltages, as shown in figure 3.13, and their output and transfer curves were more stable.

Figures 3.16a and 3.16b show the output characteristics of a nanowire FET fabricated by o-SPL and another fabricated by EBL, respectively. The curves show that both devices are *n*-channel enhancement mode transistors, *i.e.*, they have very small current levels at zero gate voltage. Both transistors present well-saturation conduction and similar current levels at the same values of source-drain and gate voltages.

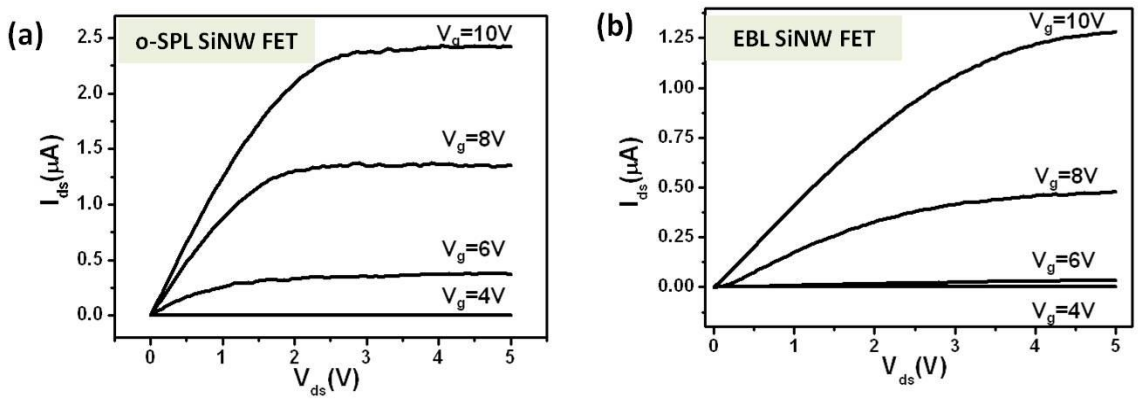

Figure 3.16 (a) Output curves of a SiNW FET fabricated by o-SPL. (b) Output curves of a SiNW FET fabricated by EBL.

The transfer characteristics in the linear region (V_{ds}= 0.5 V) on both linear and logarithmic scales of the same devices which output curves are plotted in figure 3.16a and figure 3.16b are represented in figures 3.17a and 3.17b, respectively. Once again, it can be noticed that the curves are very similar with independence of the fabrication method. The threshold voltage for the o-SPL transistor is 7 V while for the EBL transistor is 8 V. The ON/OFF current ratio is about 10^5 in both cases. The electron mobilities, calculated according to equation 3.2 with C_{nw} estimated using the trapezoidal model, are 208 cm^2/Vs for o-SPL and 200 cm^2/Vs for EBL. The small numerical differences are attributed to the different geometries of the fabricated SiNWs.

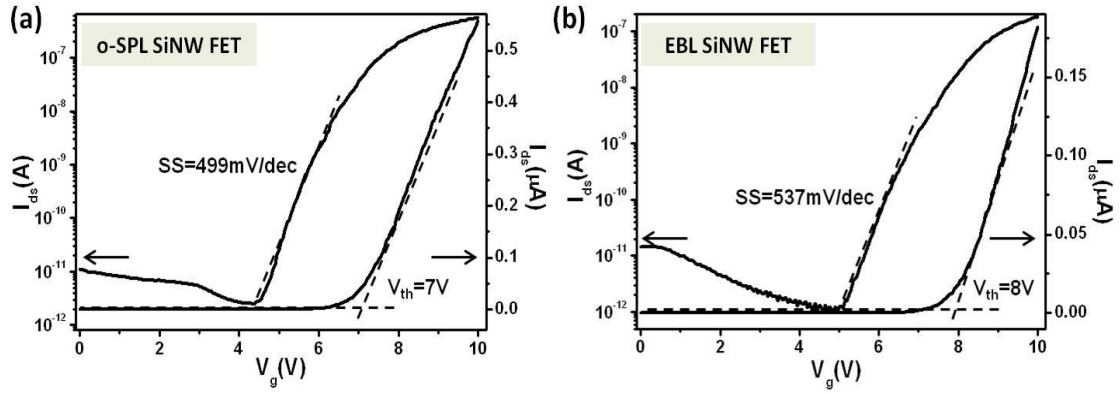

Figure 3.17. (a) Transfer curve of a SiNW FET fabricated by o-SPL in lineal and logarithmic scales. (b) Transfer curve of a SiNW FET fabricated by EBL in linear and logarithmic scales.

The subthreshold swing values obtained from the transfer curves are 499 and 537 mV/dec for o-SPL and EBL, respectively. Those values are about one order of magnitude higher than the ideal values for FETs at room temperature, 60 mV/dec. A more complete theoretical expression of the subthreshold swing than the one given in equation 3.1 is [178]:

$$SS = \ln 10\left(\frac{kT}{q}\right)\left(1+\frac{C_D}{C_{nw}}+\frac{C_{it}}{C_{nw}}\right) \quad (3.8)$$

Where C_D is the depletion layer capacitance, C_{it} is the capacitance associated with the interface trap density [191] and C'_{nw} is the gate/channel capacitance in the subthreshold regime.

Using as a first approximation the parallel plane model capacitance for C_D and C_{nw}, equation 3.8 reduces to [192]:

$$SS \approx 60mV/dec\left(1+3\frac{t_{ox}}{t_{Si}}+\frac{C_{it}}{C_{nw}}\right) \quad (3.9)$$

Considering that in these devices t_{ox} = 151 nm and approximating t_{si} with the height of the wire ≈50 nm (full depletion), we would obtain, in the ideal case of zero interfacial traps, a value of about 600 mV/dec, which is slightly higher than the values measured (~500 mV/dec) after the thermal treatment.

The above approximation does not fully apply to these devices, because of geometrical considerations. First of all, C_D is overestimated since the depletion length is comparable with the Debye length, which is of the order of 100 nm for the substrates used here. On the other hand, the value of C'_{nw} should take into account both the real geometry (trapezoidal) and the fact that, in the subthreshold regime, the nanowire-dielectric-back gate capacitance has an additional series term related with the depletion of the silicon gate electrode. Indeed, because of the relatively low doping, such depletion length is comparable with the oxide thickness. As a consequence, the role of interfacial traps in affecting the subthreshold swing cannot be neglected, even after the thermal treatment. However, the observed decrease of the subthreshold swing points out to a reduction of the density of interfacial trap states (figures 3.8a and 3.8b).

Furthermore, equation 3.9 indicates that the subthreshold swing would improve by an increase of C_{nw}, *i.e.* by a reduction of the thickness of the dielectric. This is achieved by using alternative configurations like top gate [160, 193, 194], dual gate [195], or gate all-around [161, 196]. However, those configurations pose a strong limitation towards using the nanowire transistors as sensors. Indeed, many of the top-down sensors based on SiNW FETs [169, 188] have values of subthreshold swing comparable with the ones presented in this work.

3.6.4 Comparison of the electrical properties

Table 3.2 presents the values of mobility of the nanowire transistors calculated according to the different capacitor models presented in section 3.6.2, before and after annealing treatment. Three main conclusions can be extracted from it:

- The spread of values according to the chosen capacitance model underlines the importance of considering the real configuration of the device, its geometry and the surrounding dielectrics, to estimate the transistor parameters.

- The values of the electron mobility and *SS* of the o-SPL and EBL devices are very similar after RTA treatment. For example, if we consider the mobility values calculated with the trapezoidal capacitance model, before RTA, their relative difference value is about 16%, while their relative difference reduces to about 4% after treatment. The relative differences in the *SS* before and after RTA are 12% and 7%, respectively.

  Before RTA treatment, the electron mobility and *SS* of the devices fabricated by o-SPL are worse than those made by EBL. This can be explain taking into account that the o-SPL process involves more fabrication steps, so this could have an accumulative effect in the contamination and damage of the substrate. Another reason may lie in the effect of the RIE step on the surface of the nanowires fabricated by each method: the oxide masks are 2 - 4 nm thick and are totally consumed before the end of etching. As a consequence, the unprotected silicon nanowire walls are overetched. Maybe the silicon nanowire surface/nanowire-oxide interface result more damaged in the case of o-SPL.

  However, as seen by the above results, the thermal treatment is able to reduce the imperfections originated during the fabrication steps and the electrical properties become very similar, showing that they are intrinsic properties and independent of the lithography method. The remaining differences could be explained in terms of the differences in sizes and geometry.

This conclusion can be extended to the devices fabricated by other methods in the literature, both top-down and bottom-up, represented in table 3.3. For example, from the table, it can be observed that a grown SiNW FETs [161] which uses a dielectric oxide 100 nm thick in back-gated configuration gives a *SS* of 436 mV/dec. The array of devices fabricated by nano imprint lithography [188], with dielectric oxide of 155 nm thick and back gate configuration, gives a *SS* of 550 mV/dec. These *SS* are very similar to the *SS* extracted from the devices fabricated in this chapter, where a dielectric oxide of 151 nm thick and back-gate configuration have been used.

- The previous points prove that o-SPL yields devices with good electrical properties, comparable with those in the literature. The improvement in the performance of the transistors is up to the optimization in the thermal treatment and in the design of the geometry and configuration of the device.

o-SPL		EBL	
Before RTA	After RTA	Before RTA	After RTA
μ_e (cm^2 /V·s)			
Cylindric wire on plane			
82	167	101	179
Parallel-plate			
217	444	249	413
Trapezoidal			
102	208	122	200
SS (mV/dec)			
1172	499	1031	537

Table 3.2. Electron mobility according to the different capacitance models considered in section 3.6.2 and experimental *SS* values before and after RTA treatment.

Author (reference)	Fabrication method	Gate dielectric (nm)	Channel width (nm)	μe (cm^2 /V·s)	SS (mV/dec)
Zheng *et al* [159]	Lasser-assisted catalytic growth	60 ZnO_2	20	270	300
Allen *et al* [197]	VLS growth +channel etching	200 Si_3N_4	50	175	600
Lee *et al* [161]	Low Pressure Chemical Vapor Deposition	100 SiO_2	55	2.8	436
Talin *et al* [188]	Nano Imprint Lithography	155 SiO_2	76	Not measured	550
Chen *et al* [198]	Thermal oxidation+wet etching+EBL	13.6 SiO_2	48	540	60
Huang *et al* [193]	Superlattice nanowire pattern transfer	4 SiO_2 + 6 HfO_2	10	268	168
This work	o-SPL	151 SiO_2	80	208	499
	EBL		120	200	537

Table 3.3. Electron mobility and *SS* of SiNW FETs fabricated by different top-down and bottom-up methods and the corresponding references.

3.7 Chapter summary

The main points of this chapter are:

- The o-SPL and EBL fabricated SiNW FETs have to undergo an RTA treatment in order to optimize their electrical performance (mobility and subthreshold swing) by reducing the density of trapped charges and defects originated during the fabrication process and by improving the metal-semiconductor contact.

- Both type of devices, o-SPL and EBL made, present an ambipolar behavior.

- It is important to use a capacitance model which takes into account the real geometry of the nanowire to calculate the value of the mobility.

- The values of the electron mobility and the *SS* of the o-SPL and EBL devices are very similar after RTA treatment. This means that the electrical characteristics are intrinsic properties and independent of the lithography method. The remaining differences are mainly due to the differences in sizes and geometry. This conclusion can be extended to the devices fabricated by other methods in the literature, both top-down and bottom-up.

Chapter 4

Oxidation scanning probe lithography oxide masks for pattern transfer on ultra thin silicon on insulator

The previous chapter showed that after rapid thermal annealing treatment, the silicon nanowire field effect transistors fabricated by oxidation scanning probe lithography have good electrical properties, comparable to those fabricated by other top-down and bottom-up methods. The back gate configuration of the device and the thickness of the dielectric layer are the main elements which control the value of the subthreshold swing. A further decrease in the transistor channel size and the subthreshold swing could improve the sensitivity and the performance of the SiNW FETs as nano sensors. The use of a silicon on insulator substrate with thinner top silicon and dielectric layers is proposed in this chapter to accomplish the above targets while keeping the back gate configuration. Here we use a SOI with a silicon top layer of 12 nm and a BOX of 25 nm. In this way, in the vertical direction, the size of the silicon nanowire is already reduced almost a factor of five from the beginning.

With respect to the fabrication steps, the pattern transfer by reactive ion etching have to be optimized, because it requires the transfer of very thin masks (0.5-1 nm) into a very thin silicon layer (12 nm) in a controlled and reproducible way. In this chapter, a method to obtain 12 nm thick silicon nanowires by using silicon oxide masks of about 1 nm high is described. The etching gas is SF_6 with a certain amount of oxygen to passivate the exposed SiNW sidewalls and to enhance the selective etching of Si versus the mask and the radio frequency power (*rf*-power) and chamber pressure are chosen to minimize the ion density and hence, to favor chemical processes versus sputtering removal. This method produces silicon nanowires that keep the width of the initial oxide mask and enables the fabrication of silicon nanowires with cross-sections below 100 nm^2. Those transistor channel sections are among the smallest obtained with a top-down lithography method [199-201].

Regarding to the electrical performance of the devices, two main issues arise from the use of an ultra thin SOI substrate:

- The decrease in the thickness of the dielectric layer increases the leakage paths through the dielectric layer and therefore, the leakage current from the back gate.

- As the silicon nanowire cross section gets smaller, the resistance of the channel increases according to Ohm's law, so the geometry of the devices, for example, the length of the transistor channel, or the metal electrodes used for the fabrication of the FETs in chapter 3 have to be changed.

Some of the possible prospects to achieve working transistors are explained at the end of the chapter.

4.1 Pattern transfer process from 1 nm high oxide mask into 12 nm thick Si layer

4.1.1 Reactive ion etching

Wet etching is still the method of choice for several processes at the batch level such as the fabrication of AFM tips and micromachining due to its low set-up requirements and low cost. However, in many fabrication processes at the nanoscale, which requires the pattern transfer of features with specific geometries and small sizes, the use of reactive ion etching (RIE) is preferred because it offers control over the etching directionality without depending on the crystal orientation of the surface to be etched and allows more control over the selectivity, the etching rate and the cleanliness during the process.

RIE is a dry etching technique which has a combination of physical and chemical etching mechanisms [202-205]. The physical mechanisms are associated with ion milling/sputtering and yield an isotropic etching. The chemical mechanisms favor the anisotropic etching by the action of chemically reactive atoms and radicals. By adjusting the parameters involved in the process, such as the chamber pressure, temperature, *rf*-power or gas composition, is possible to make one of the mechanisms- the physical or the chemical- dominant over the other. This is normally monitored by the ion energy flux to neutral flux ratio.

The RIE system consists in a parallel plane capacitor reactor (figure 4.1), so it is alternatively called capacitively coupled plasma (CCP). The sample is placed in the lower electrode and the etching gas or gas mixture is introduced in the chamber. Then, a glow discharge decomposes the feeding gas generating different species such as neutrals, electrons, radicals, photons and ions. The reactive species are directed from the bulk plasma to the electrode where the sample is placed by diffusion/convection. Then this reactive species adsorb in the surface, react with it and produce volatile species that desorbs from the surface. During the process, the continuous ion milling is useful if, for example, the etching and passivating steps are performed simultaneously, since it helps to remove the passivation layer which is forming on the surface walls and keeps on generating 'etching sites'.

The main disadvantage of RIE is that is a process where many variables have to be controlled. Moreover, the minimum variation in these variables can affect the etching process, making difficult the reproducibility of the results [204, 206].

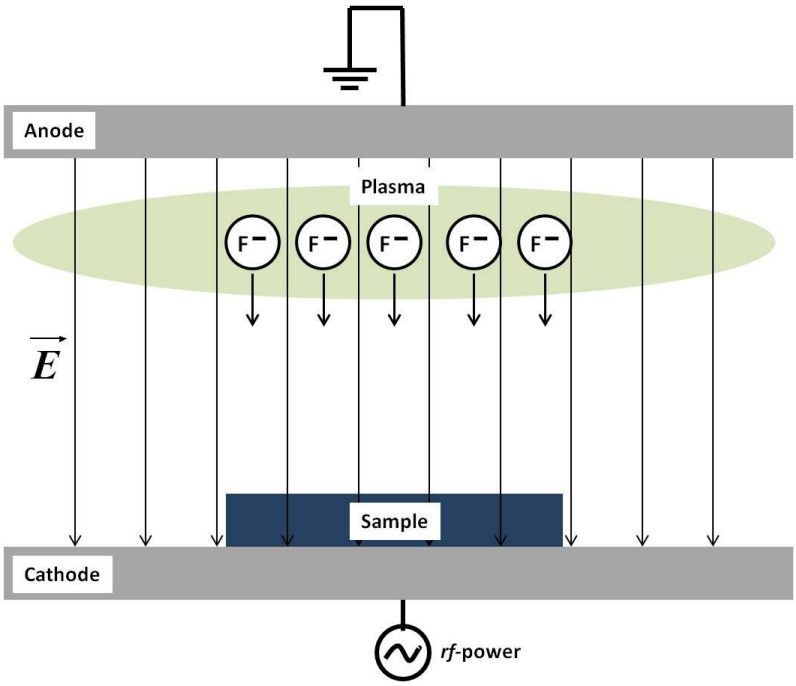

Figure 4.1. Scheme of reactive ion etching. The parallel plane reactor electrodes create an electric field which drives the accelerated ions towards the sample to etch.

4.1.2 Experimental set up

The silicon oxide masks and the transferred silicon nanowires were made on ultra thin silicon on insulator substrates (MEMC/SunEdison, US). The top (100)-oriented Si layer is 12 nm thick, *p*-doped and has a nominal resistivity of 9-15 Ω•cm. The buried oxide layer (BOX) has 25 nm of thickness. Markers made of metal pads were defined on the SOI substrate by photolithography and metal evaporation to locate the different patterns during the fabrication and characterization steps. The substrates underwent the cleaning protocol explained in chapter 2.

The o-SPL was performed by operating the AFM in the amplitude modulation mode with a free amplitude in the 5-10 nm range and a set point amplitude/free amplitude ratio of about 0.9. The relative humidity was kept in the 40-60% range. Voltage pulses of 15-30 V amplitude and 0.5 ms duration were used. The height and width of the silicon nanowires were characterized by the cross sections from the AFM topographic images of the patterned structures taken after their fabrication. The silicon oxide mask height and width (FWHM) are, respectively, about 0.3-2.5 nm and 20-60 nm.

In the chapter, the thickness of the silicon nanowires is used to refer size in the vertical direction. However, for the oxide masks, height is used instead of thickness, because only the portion of the oxide grown over the surface is considered.

The etching experiments were performed in the reactive ion etching system PlasmaLab 80 (Oxford Instruments, UK), which has a frequency of 13.56 MHz. The RIE process for each patterned substrate involved several preliminary steps. Once the sample is introduced in the chamber, the pressure is lowered to 10^{-8}Torr for 1h. Then there is a purge with N_2 for 1 min. This step is followed by another vacuum cycle at 10^{-8} Torr for 5 min. Then the SF_6:O_2 gas mixture is introduced and let to stabilize for 1 min at the specific chamber pressure of the experiment.

4.1.3 Adjustment of the etching parameters

The parameters of reactive ion etching such as *rf*-power, chamber pressure, gas composition or gas flow have to be tuned to promote a chemical and anisotropic etching process instead of a sputtering and isotropic etching process. The selectivity of the SiO_2 mask/Si surface etching has to be maximized because the etching of a 12 nm thick layer requires an etch rate slow enough to have a good control over the process.

The value of the chamber pressure was adjusted to minimize the ion current density and then, the SF_6:O_2 ratio to have a relatively high concentration of F and some O. The presence of F favors the chemical etching of the silicon while the presence of O helps to passivate the emerging silicon sidewalls slowing down the etching there.

The sidewall of the oxide masks fabricated by o-SPL has a small angle with respect to the horizontal plane, being 4º a typical value. As a consequence, the masks erode during the etching at a certain rate. The experiments performed to adjust the etching parameters produced three different pattern transfer situations with respect to the starting point (figure 4.2a) that served as a guide to determine the optimized values:

- The ideal case (figure 4.2b) refers to the production of SiNWs which conserves the 12 nm thickness of the initial silicon layer, which means that the oxide mask or a part of it resisted during the etching time protecting the underneath silicon.

- The structure called underetched (figure 4.2c) corresponds to the remaining of the whole silicon thickness protected by the mask and a certain thickness of the unprotected silicon after the end of the etching process.

- The opposite case to the previous one is the overetched structure (figure 4.2d), which is produced when the whole oxide mask is consumed before the etching has stopped. Part of the silicon underneath the mask has been etched.

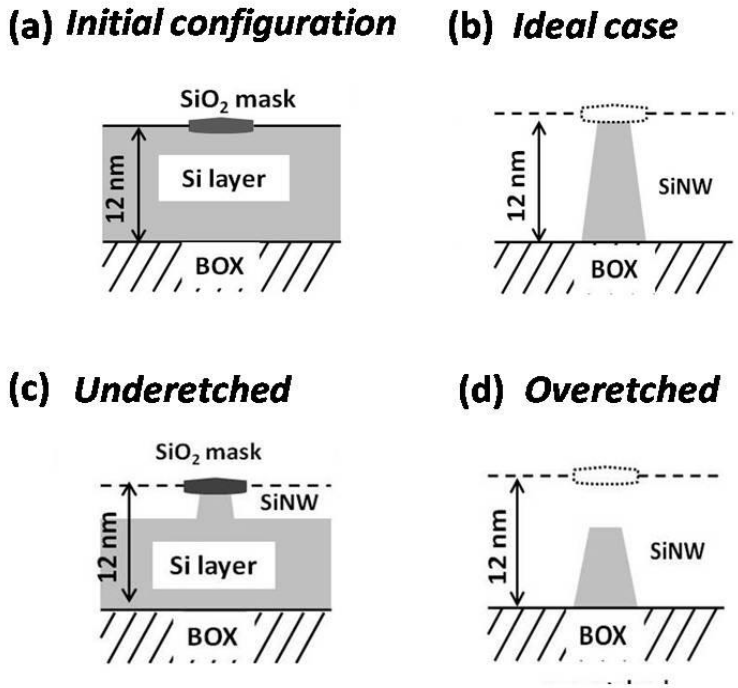

Figure 4.2. Scheme of the possible resulting patterns after different etching conditions. (a) The initial situation of the oxide mask/silicon layer. (b) The ideal etching case is that which produces SiNWs 12 nm high, the initial thickness of the SOI top layer. (c) The underetched structure corresponds to the whole silicon thickness protected by the mask and a certain thickness of the unprotected silicon. (d) In the overetched case, part of the silicon underneath the oxide mask has been etched.

- The ***rf*-power** value was chosen low to minimize the physical etching and the etching rate [203]. For the RIE instrument used in this work, 10 W was the minimum value which formed a stable plasma sheath.

- The **chamber pressure** was adjusted in order to minimize the ion density, responsible of the milling aspect of the etching. The studied range of values was 20-90 mTorr. Figure 4.3 shows the thickness of the resulting SiNW as a function of the chamber pressure for fixed values of *rf*-power, gas mixture ratio and etching of, respectively, 10 W, SF_6:O_2 (12:3) sccm and 126 s. Only under the maximum pressure allowed by the RIE instrument used in this work, 90 mTorr, the original thickness of the active Si layer was conserved in the etching process. For lower pressures, the thickness of the SiNW decreased monotonically with decreasing the pressure because the o-SPL masks were consumed during the etching cycle (126 s); hence all the structures produced for these values were overetched (figure 4.2d). This is because in the pressure range of 0 to 100 mTorr, the lower the pressure the higher the ion flux and the lower the concentration of F. This implies that sputtering dominates over the chemical etching. This mechanism reduces the etching selectivity [207].

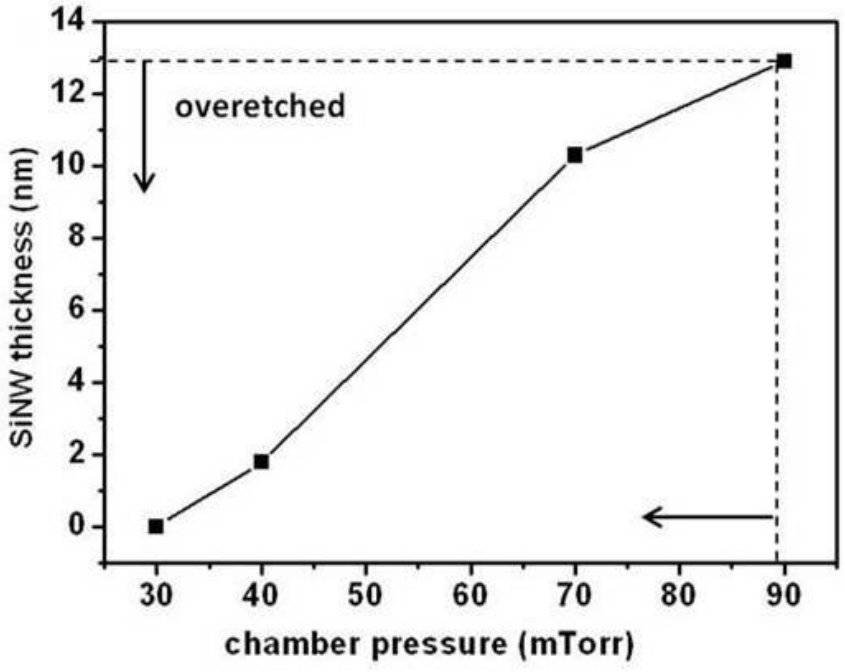

Figure 4.3. SiNW thickness as a function of the chamber pressure. Only in the case of 90 mTorr, the produced SiNWs preserve the original thickness of the silicon layer. For lower chamber pressures, the produced structures are overetched.

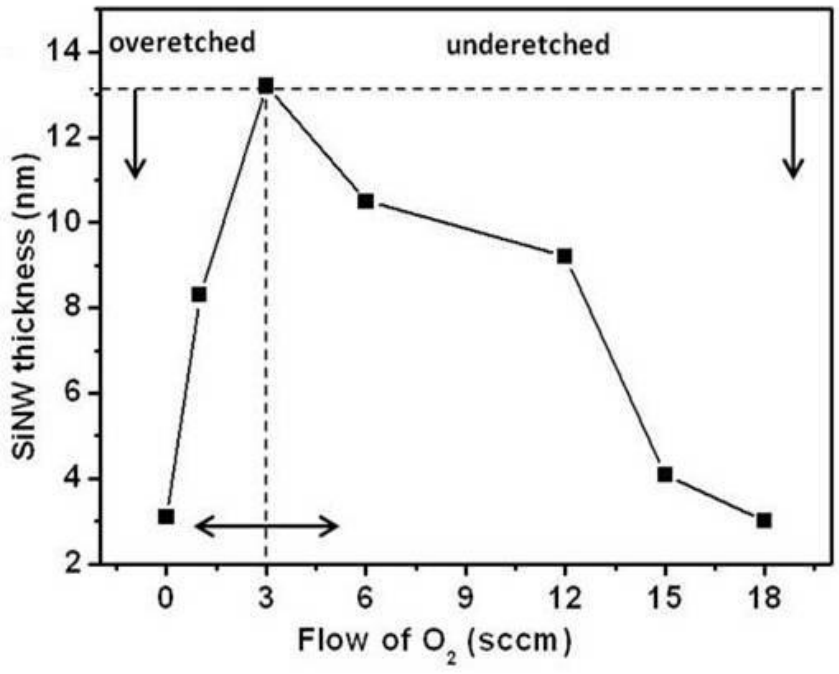

Figure 4.4. SiNW thickness as a function of the oxygen flow. For a fixed flow of SF_6, there is a peak O2 flow value of 3 sccm at which the produced SiNWs preserve the original thickness of the silicon layer. At lower oxygen flows, the resulting structures are overetched. At higher oxygen flows, the produced structures are underetched.

Each data point shown in figures 4.3 and 4.4 represent an average taken over 5-10 different SiNW structures and silicon oxide masks fabricated under similar o-SPL conditions.

- The main gases used for the SiO_2 mask/Si substrate system are the fluorine-based ones such as the SF_6 because they give faster etching rates than the other halogen gases. However, the etching of silicon with **SF_6** needs the addition of an inhibitor to passivate the sidewalls of the features during the process because is quite aggressive. The main passivating gases used are **O_2** [207-210] and C_4F_8 [201, 211-212]. In this work, oxygen was employed as the passivating gas. The proportion of oxygen to find the optimum selectivity between the oxide and the silicon was found by varying the oxygen flow at a fixed SF_6 flow. Figure 4.4 shows the evolution of the SiNW thickness as function of the O_2 flow, for fixed values of chamber pressure, SF_6 flow, *rf*-power, and etching time of, respectively, 90 mTorr, 12 sccm, 10 W and 126 s. The data shows a maximum at 3 sccm, which implies that the original Si layer under the o-SPL mask was preserved during the etching (figure 4.2b). At lower oxygen flows, the Si layer under the mask was overetched (figure 4.2d). On the other hand, at higher flows the resulting silicon structures were underetched (figure 4.2c). The observation of a maximum in the etching rate as the oxygen is increased has been reported for the etching of other structures and materials [208, 209, 213-214].

The SF_6:O_2 ratio is used to modulate the F concentration with respect to the O concentration because in the range of SF_6-to-O_2 ratios used here, the ion current density remains practically constant. Consequently, the competition between F and O to react with Si can be described by the following reactions [215]:

Passivation reaction: $$Si + xF + yO \rightarrow SiF_xO_y \quad (4.1)$$

Etching reaction: $$Si + 4F \rightarrow SiF_4 \quad (4.2)$$

Oxidation reaction: $$Si + 2O \rightarrow SiO_2 \quad (4.3)$$

The SiF_4 are the volatile products that form when the F atoms react with the silicon surface and SiF_xO_y is the sidewall passivation layer. The probability of F to react with SiO_2 is two orders of magnitude smaller than with Si. Consequently, by changing the oxygen flow is the etching rate of Si what is affected [216].

A study of the thickness of the SiNW as a function of the height of different o-SPL oxides was performed (figure 4.5). The etching conditions were 10 W of *rf*-power, 90 mTorr of chamber pressure, a gas mixture of SF_6:O_2 (12:3 sccm) and an etch time of 126 s. The intersection point of figure 4.5 shows that an o-SPL mask of 1.1 nm in height enables the transfer of a 12 nm thick SiNW, this is, the thickness of the nanowire that matches the

thickness of the Si layer of the SOI (figure 4.2b). This means that the Si under the mask has not been removed during the process. It also implies that the whole oxide mask has been removed. By reducing the oxidation voltage from 21 V to 15 V, the oxide mask height changes from 1.1 nm to ~ 0.3 nm. By using oxide masks with a height smaller than 1.1 nm and applying the above etching conditions, sub-12 nm SiNW down to 2 nm can be fabricated. This implies that SiNWs of cross-sections below 100 nm^2 (3x30 nm^2) could be fabricated. Those values are among the smallest Si nanowire cross-section fabricated by any top-lithography.

In chapter 2, the o-SPL oxide was shown to grow above and below the Si baseline. The inset in figure 4.5 represents the AFM cross-section of one of the o-SPL masks before and after its etching in HF. Only the oxide height, this is, the oxide that protrudes from the Si baseline is considered for these experiments.

Each data point from figure 4.5 represents an average taken over 10 oxide masks with the same height and their resulting SiNWs after etching.

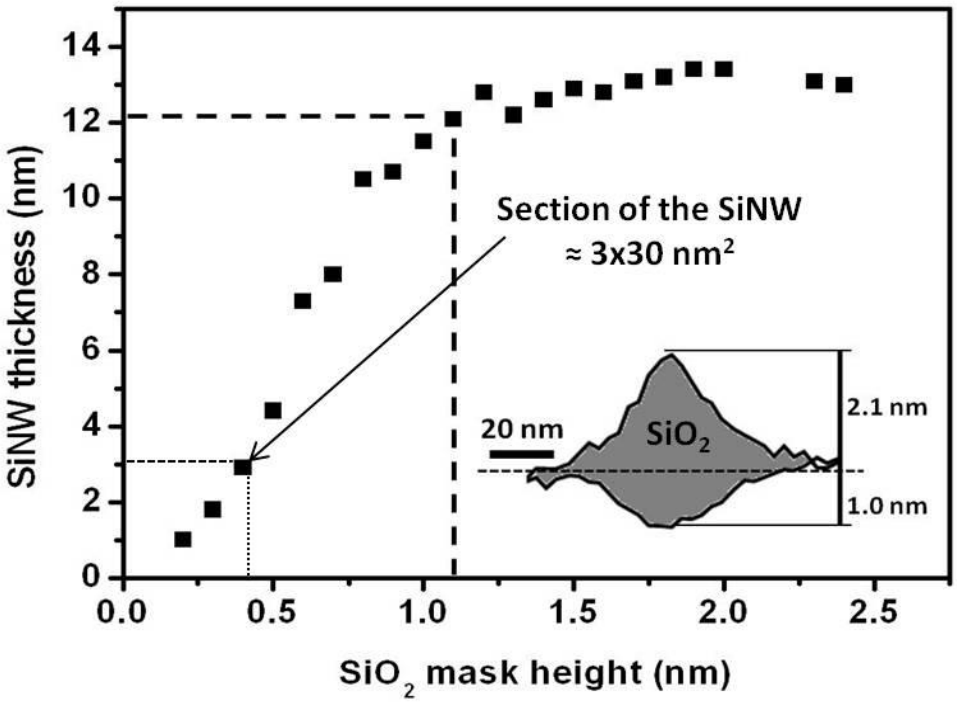

Figure 4.5. Thickness of the silicon nanowires as a function of the height of the oxide masks (measured from the substrate baseline). The dotted line shows the value of the oxide height that generates a SiNW with a thickness identical to the active Si layer of the SOI. The inset shows the structure of the oxide mask fabricated by o-SPL. It shows that the oxide grows above and below the Si baseline.

The selectivity of this process is estimated from the angles of the mask ($\tan\theta_{nw}$) and the transferred SiNW ($\tan\theta_{mask}$) with respect to the horizontal plane by using the expression [215, 217-218]:

$$S = \frac{\tan\theta_{nw}}{\tan\theta_{mask}} \qquad (4.4)$$

Figure 4.6 shows the cross-sections and AFM images of an o-SPL mask (figure 4.6a) and its corresponding SiNW (figure 4.6b) after etching under the conditions determined to preserve the initial thickness of the Si layer. By applying equation 3.4 to a series of masks and their resulting Si structures similar to the represented in figure 4.6, we obtain selectivity with an average value of 11.

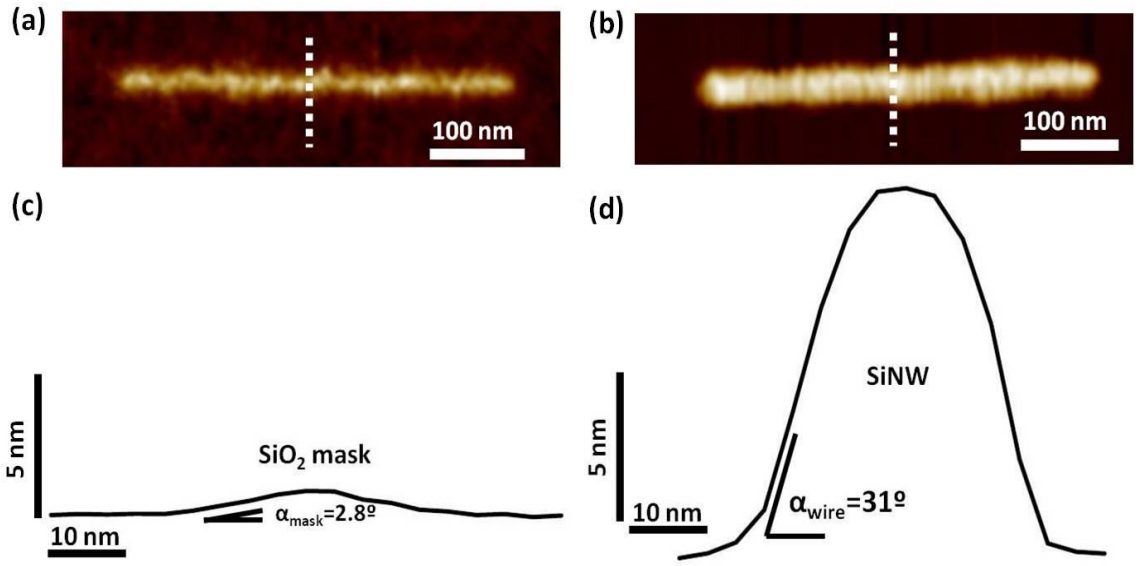

Figure 4.6. (a) AFM image of an oxide mask 1.1 nm high. (b) AFM image of the silicon nanowire after the optimum etching process described in the text was applied to the mask shown in (a). (c) AFM cross section of the oxide mask shown in (a). (d) AFM cross section of the SiNW shown in (b). Both cross-sections are at the same scale.

Figure 4.7 shows the AFM topographic images and cross-sections of an array of silicon oxide masks with similar heights (1.1-1.4 nm) and the corresponding silicon nanowires after the etching. The widths and heights of these structures are compiled in table 4.1. Taking into account the effect of the AFM tips on the lateral measurements, the SiNW:oxide mask width ratio is close to 1. This means that with this process is possible to obtain nanowires which widths are determined by the width of the masks fabricated by o-SPL.

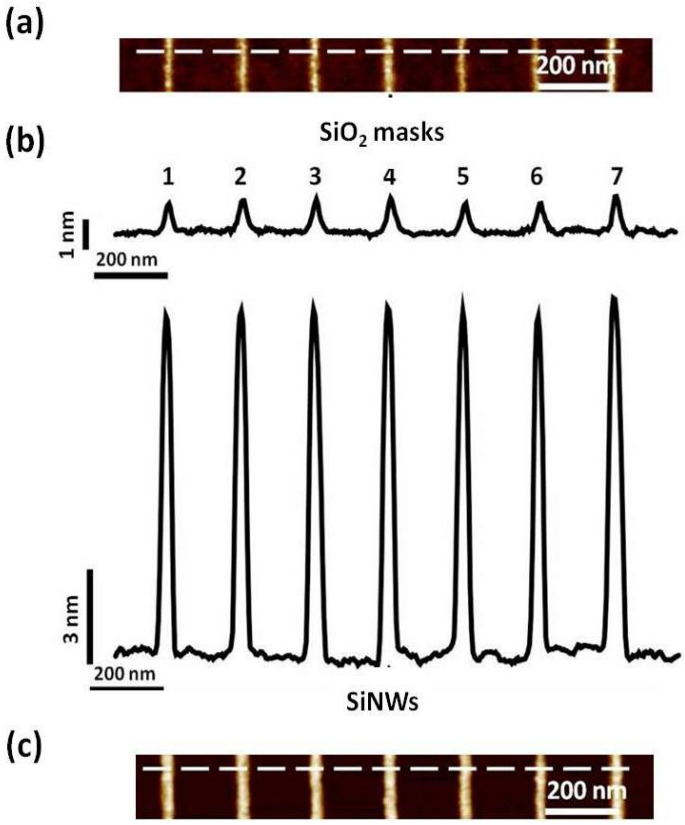

Figure 4.7. (a) AFM image of an array of o-SPL oxide masks with similar heights. (b) AFM cross sections of the oxide masks shown in (a) and the resulting SiNWs after etching shown in (c). AFM image of the produced array of SiNWs using the array of masks shown in (a).

№	h(nm)		w(nm)	
	SiO_2 mask	SiNW	SiO_2 mask	SiNW
1	1.1	12.7	24	27
2	1.1	13.0	24	34
3	1.3	13.0	34	35
4	1.4	13.1	33	30
5	1.2	12.9	35	33
6	1.1	12.7	29	24
7	1.4	13.5	25	39

Table 4.1. Heights and widths (FWHM) of the silicon dioxide masks and silicon nanowires labeled 1-7 in Figure 4.7.

To summarize this section, the optimal parameters for the RIE process are found to be a *rf*-power of 10 W, a chamber pressure of 90 mTorr, and a gas mixture of SF_6:O_2 (12:3) sccm, during an etch time of 126 s. The highlights of this process are:

- It is an etching process where there is no need of a resist mask.
- With standard parameter values for the etching of SiO_2 mask/Si surface, selectivity of about 11 is achieved.
- The ratio of the oxide mask width and the silicon nanowire width is close to 1, so it fulfills the requirement of a pattern transfer process that keeps the lateral resolution given by o-SPL.
- It is possible to obtain SiNWs with very small cross sections (<100 nm^2).

4.1.4 Examples of etched silicon structures with the optimized process

In this section, some of the structures that can be fabricated by the combination of o-SPL and the RIE process described in this chapter are shown.

All these structures were fabricated with the same etching conditions.

For the sake of simplicity, the o-SPL conditions to fabricate the oxide masks in each case are given as: pulse voltage, oxidation time, relative humidity and free amplitude, always in the same order.

- Array of nanowires

The array of nanowires with the minimum pitch resolved after the etching process was found to be 40 nm, represented in figure 4.8a. The oxide masks that produced the SiNWs of this array had a height about 0.5 nm and were fabricated under the oxidation conditions of 15V, 0.5 ms, 46% and 5 nm. The widths (FWHM) of these SiNWs are about 25 nm. The SiNWs inside the array have heights about 4 nm, while the silicon nanowires located at the opposite ends have heights about 8 nm with respect the surface baseline. This is because the initial oxide masks overlap each other, so inside the array, the etching is not complete. The pitch of the array of 25 SiNWs represented in figure 4.8b has a pitch of 50 nm. The oxide masks were 0.5 nm high and were fabricated under the oxidation conditions of 18V, 0.5 ms, 46%, 5 nm. These SiNWs have widths about 30 nm at FWHM. In this case, the height of the SiNWs inside the array is about 5.5 nm, while the height of the SiNWs located at the opposite ends is about 8 nm.

These results show that it is possible to have a dense array of SiNWs. This configuration could be used for biosensing applications, since there is much area/volume ratio of nanostructured silicon available.

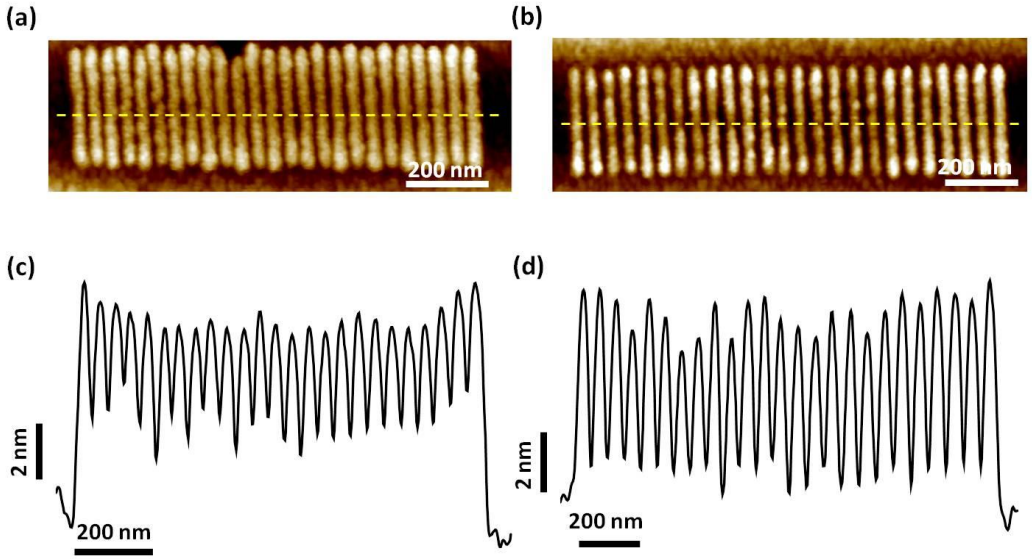

Figure 4.8. (a) AFM image of an array of 25 SiNWs with a periodicity of 40 nm. (b) AFM image of an array of 25 SiNWs with a pitch of 50 nm. (a) AFM cross section of the array shown in (a). (d) AFM cross section of the array shown in (b).

- Nanopillars

It is possible to make an array of vertical nanowires by defining a matrix of oxide dots with a chosen periodicity. In figure 4.9a, it is represented a matrix of 20x20 SiNWs with a periodicity of 100 nm, from a starting matrix of 20x20 oxide dots, with heights of 0.5-0.8 nm, fabricated under the oxidation conditions of 15V, 0.5 ms, 42% and 5 nm. These nanopillars have an average height of 8 nm and widths at FWHM between 30-50 nm.

This result shows the potential of the o-SPL to make an ordered array of sub-50 nm width vertical SiNWs with capability to chose the location of the features and their periodicity. This array of pillars could be exploited in photonic or optoelectronic applications. Moreover, for this purpose, it could be possible to explore the possibility to make by o-SPL etching masks different from silicon oxide to obtain nanopillars of III-V semiconductors. For example, the performance of local oxidation on GaAs has already been performed [119-121].

- Crossed nanowires

It is also possible to transfer crossed oxide line masks into the silicon. In figure 4.9b, an array of 10 SiNWs overlapped over 10 SiNWs with a rotation of 90º is represented. Their widths (FWHM) are about 40 nm. The SiNWs of the bottom array have heights about 4-7 nm. The SiNWs of the top array have heights about 8-9 nm. The initial oxide masks were fabricated under oxidation conditions of 15V, 0.5 ms, 40% and 5 nm. Their heights were about 0.3-0.6 nm.

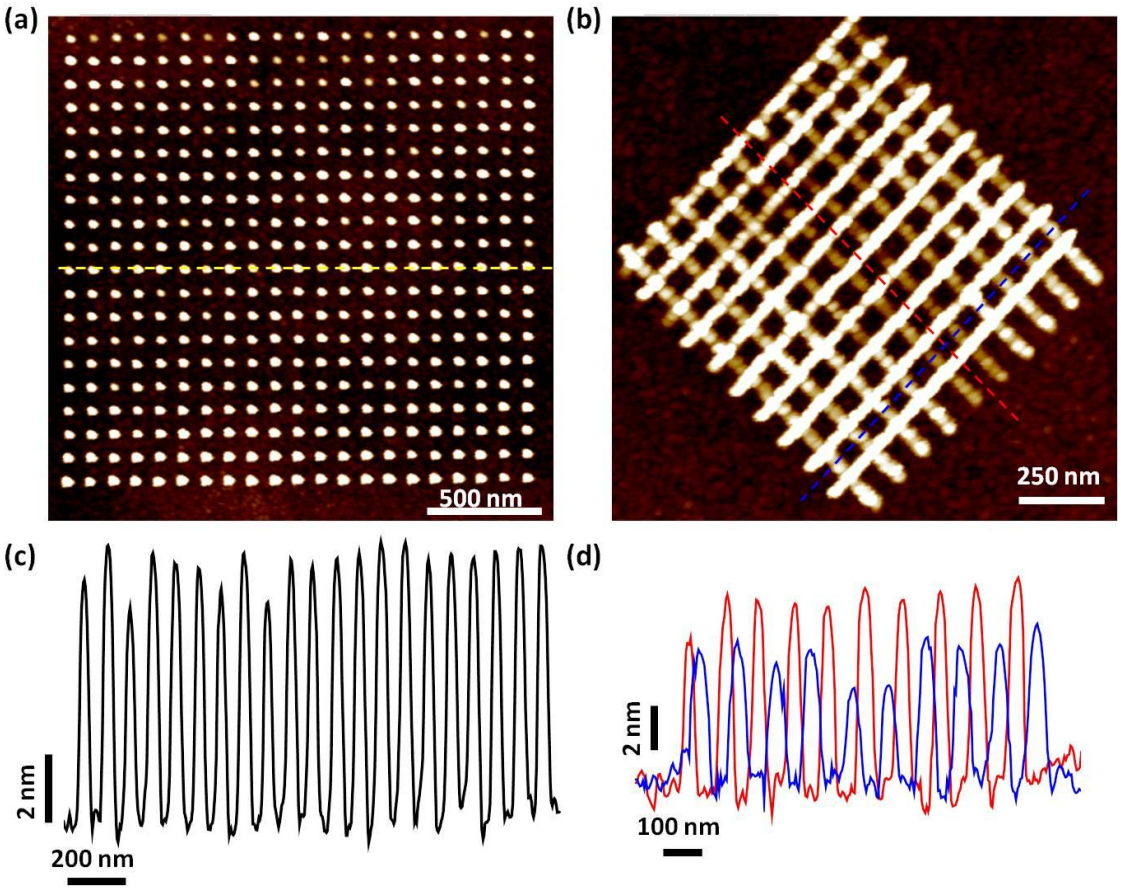

Figure 4.9. (a) AFM topographic image (top) of a 20x20 matrix of vertical SiNWs with a periodicity of 100 nm. (b) AFM topographic image of an array of crossed SiNWs. (c) AFM cross section of the array of nanopillars marked with the yellow dashed line in (a). (d) AFM cross sections of the areas marked with the red and blue dashed lines in (b).

4.2. Issues on the conduction of the o-SPL SINW FETs fabricated with the UT-SOI substrates and prospects for future work

The o-SPL SiNW FETs fabricated by the process described in chapter 3 using the ultra thin SOI present two main issues:

- The increase in the leakage current contribution from the back gate through the dielectric due to the decrease in the thickness of its layer: 25 nm instead of the 151 nm which the oxide layer of the previous SOI had.

- The nanowires become more resistive as a consequence of the decrease in the size of the transistor channel section.

The steps to address the above issues are:

- To study the leakage level through the dielectric layer, beginning from the SOI wafer and reducing the area of the top silicon layer consecutively.

- To study the influence of the transistor length on the conduction of the nanowires. According to Ohm's law:

$$R = \rho \frac{L}{A} \qquad (4.5)$$

  The resistance is inversely proportional to the section of the channel. Thus, the length of the transistor has to be reduced (up to now, they were made in a range of 5 μm-10 μm), but stopping at the value when short channel effects start to appear [178]. The photolithography step to contact the nanowire with the electrodes (chapter 3, section 3.1) is replaced by EBL.

- To change the metal used to make the electrodes and find the corresponding rapid thermal annealing treatment for this new metal/nanowire contact. Currently, Cr/Au is being used and the SiNW FETs fabricated with the previous SOI present an ambipolar behavior. For example, according to Koo *et al* [183], Ti has a lower Schottky barrier height for electrons than Cr. Additionally, the Ti can formed a silicide by annealing treatment at mild temperatures [219], so the use of Au can be kept to make SiNW FETs with Ti/Au metal contacts.

- To fabricate an array of n transistors with similar lengths and sections (resistances in parallel configuration).

4.3 Chapter summary

The main points of the chapter are:

- By using a SOI with silicon top layer of 12 nm, the size of the silicon nanowire is reduced almost a factor of five in the vertical direction from the beginning.

- By applying RIE to o-SPL oxide masks of 1 nm high at an *rf*-power of 10 W, a chamber pressure of 90 mTorr, and a gas mixture of SF_6:O_2 (12:3) sccm, SiNWs which preserve the thickness of the Si layer and the width given by the oxide mask are achieved.

- With the combination of o-SPL and RIE, it is possible to obtain SiNWs with very small cross sections (<100 nm^2).

Chapter 5

Oxidation scanning probe lithography applications: Hybrid nanowire-nanoparticle photodetectors and 2D electronic devices

In this chapter, two concrete examples where the o-SPL technique has been used to fabricate functional devices are presented: Hybrid nanostructure photosensors and MoS_2 thin film-based transistors.

5.1 Hybrid Au NPs-SiNW FET photodetector

Section 5.1 presents the use of o-SPL SiNW FETs decorated with functionalized Au NPs as sensitive and selective photodetectors. This work is being developed in collaboration with Prof. Francesco Stellacci research group, SUNMIL, at EPFL, Lausanne.

5.1.1 Introduction

In the last years, the nano devices are expected to be multifunctional, that is, one same nanostructure having different functions or a combination of nanostructures for a specific functionality [220]. One example is the use of nanowires decorated with nanoparticles. Each nano system has its own properties and it is used for different applications, but when they are used together, the sum of their contributions gives an enhanced performance for a determined application. Some of the recent examples of these hybrid nano devices are:

- The combination of the Ag NPs with SiNWs for biomedical applications [221]. Ag NPs are interesting for medical applications because they present antibacterial activity and they are not very invasive to human cells. However, one of the issues to use them is that their easily aggregates, and thus, the loss of their properties cannot be avoided. The Ag NPs decorated in the wall of the silicon nanowires present more resistance to aggregation, so their antibacterial effect is longer and more stable.

- The combination of the Au NPs and SiNWs to fabricate a plasmonically enhanced photocurrent detector [222]. This configuration takes advantage of the ability of the Au NPs to activate plasmonic resonance modes and the high surface/volume ratio that SiNW offers.

- Free-label SiNW biosensors decorated with Au NPs [223]. The Au NPs can be functionalized with thiol groups. By this way, the DNA can be immobilized more easily with the help of the NPs and the sensitivity of the binding events is enhanced.

5.1.2 Components of the hybrid nanodevice

- Three different gold particles functionalized with cetyltrimethylammonium bromide (CTAB) were used to make the experiments: spherical nanoparticles with an absorption maximum at 520 nm, and two different nanorods with absorption peaks at 800 nm and 1400 nm and aspect ratios of 4 and 9, respectively. These NPs were purchased from Nanopartz™ Inc (US). A scheme of the different nanoparticles is represented in figure 5.1.

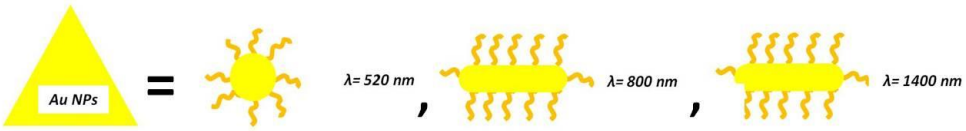

Figure 5.1. Scheme of the three types of CTAB-Au NPs used for the experiments.

- Macro FETs (figure 5.2a) fabricated from the lightly boron doped 57 nm-thick Si and 151 nm-thick SiO_2 layer SOI, with gold contacts and back gate configuration. Through the text, they are referred as flatFET.

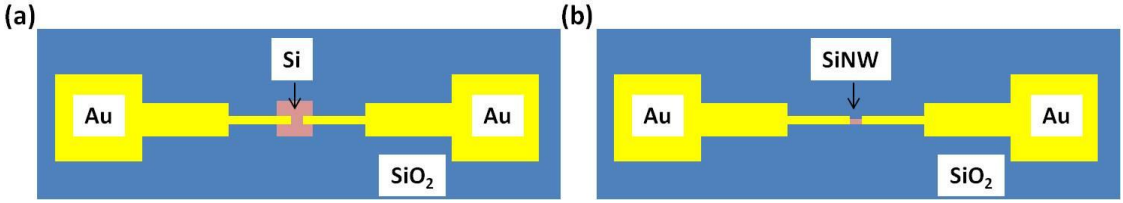

Figure 5.2. (a) Scheme of a flatFET. (b) Scheme of a nanoFET. The devices are exactly the same except the size of the transistor channel. In the case of the flatFETs, the silicon area is in the order of millimeters. In the case of the nanoFETs, the transistor channel is a SiNW.

- The o-SPL SiNW FETs (figure 5.2b) are fabricated with the process described in chapter 3 using the same SOI as to fabricate the flatFETs. Figure 5.3a shows the AFM phase image of a typical device with L= 6 µm, W = 165 nm and t = 50nm. These devices are referred as nanoFETs in opposition to the flatFETs.

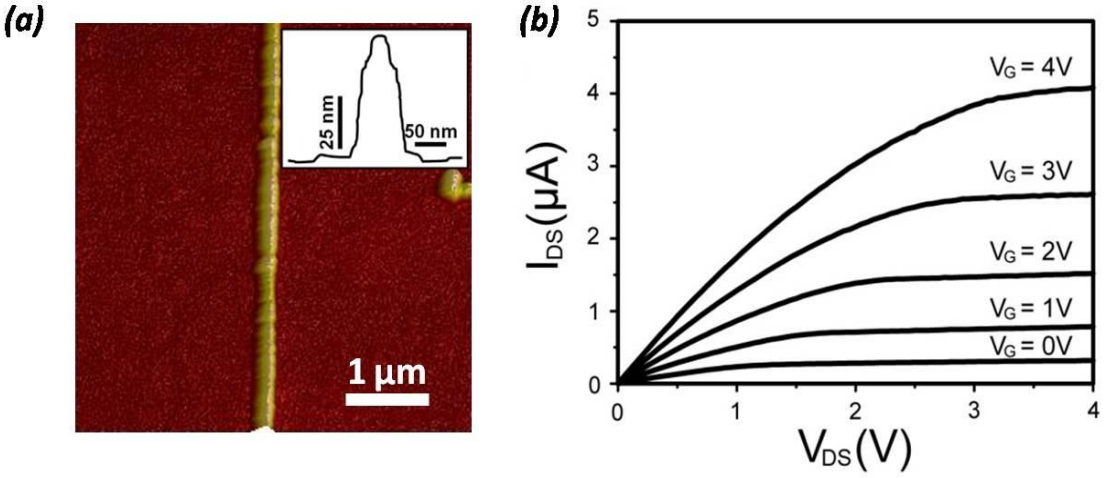

Figure 5.3. (a) AFM topographic image and (b) output curve of a typical SiNW FET used in the photodetection experiments.

The particles were deposited onto the nanowire by drop-casting. A SEM image of a device consisting in the SiNW FET coated with the Au NPs is shown in figure 5.4.

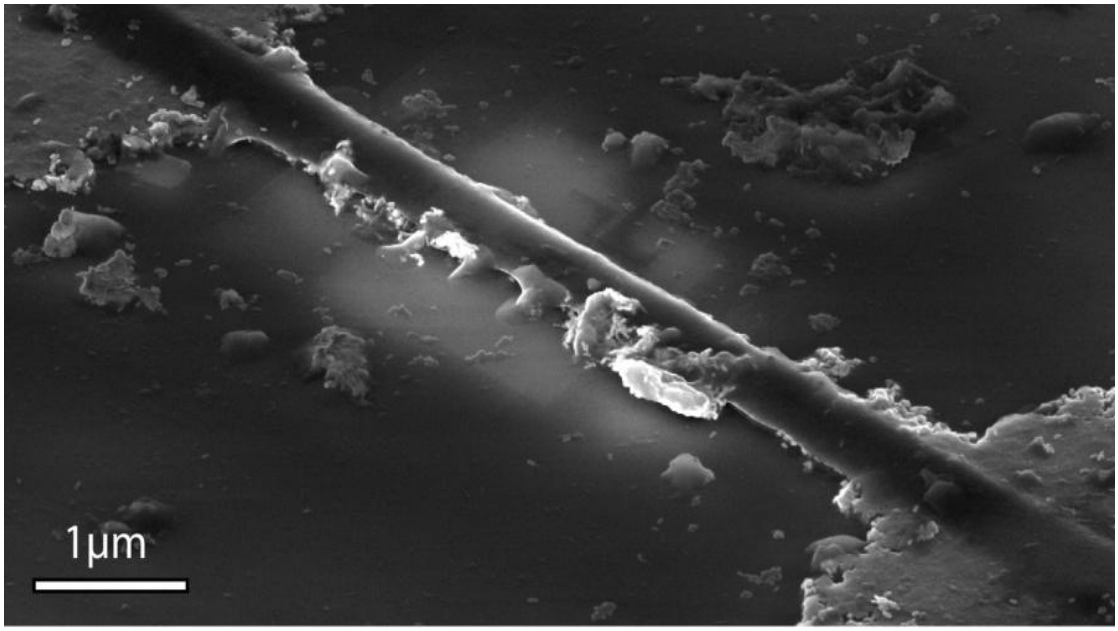

Figure 5.4. SEM image of a SiNW FET coated with the (800 nm) CTAB-Au nanorods.

5.1.3 Experimental set-up

To study the photoresponse of the SiNW FETs coated with the Au NPs under illumination, the experiments consisted in a **laser** focused to a spot of about 15 μm in diameter on the device through a **pinhole mask**. **Multi-axis motorized stages** allowed the beam to be positioned on the sample with high spatial precision. For the **laser sources**, three different fiber-coupled laser diodes of 532 nm, 808 nm and 1550 nm with adjustable power by current controller were used. The illumination intensity was calibrated by an **optical power meter** (PM 100D with sensors S120C and S122 C, Thorlabs, Germany). All the measurements were performed in a dark and shielded enclosure under ambient conditions at room temperature. Current-voltage characteristics were carried out in a **probe station** using either an Agilent parameter analyzer (4155C) and a N5230 network analyzer or a Hewlett-Packard analyzer, (HP4145B). For current-time measurement, laser beam was modulated with a **beam shutter** (Lambda SC). A scheme of the experiment is represented in figure 5.5.

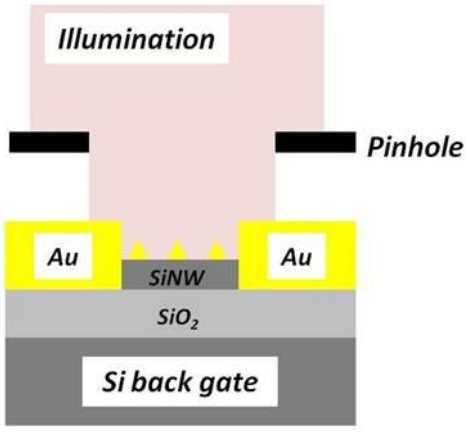

Figure 5.5. Scheme of the SiNW FET + CTAB-Au NPs device under illumination.

5.1.4 Photosensing results

The photoresponse of the devices is measured from the changes in the drain-source current under dark-illumination cycles and is defined as:

$$\textit{Photoresponse}(\%) = \frac{I_{dark} - I_{illumination}}{I_{dark}} x100 \qquad (5.1)$$

The sign of the photoresponse is different for flatFETs and nanoFETs when they are illuminated, as observed in figure 5.6. Under illumination with the 808 nm laser spot, the flatFET show an increase in the photocurrent due to the increase of carrier numbers. In the case of a nanoFET (without particles), the photocurrent shows the opposite behavior. This negative photocurrent observed in the nanoFET probably originates at the semiconductor-metallic contacts established between the nanowires and gold electrodes.

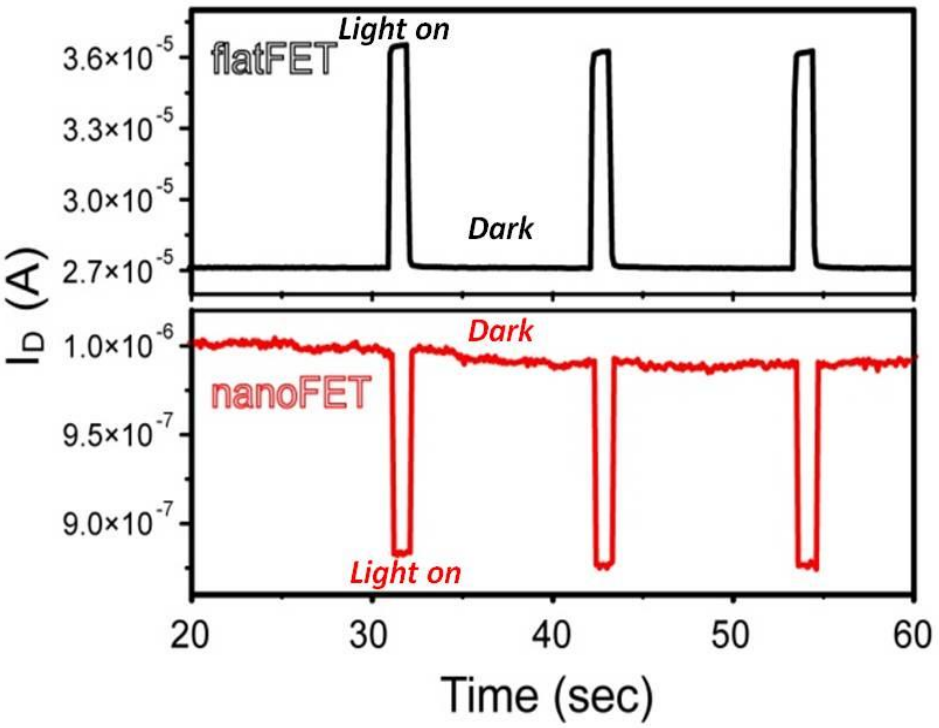

Figure 5.6. I(t) curves showing the device response under dark and illumination cycles for a flatFET (top graphic) and a nanoFET (bottom graphic). The sign of the photoresponse is opposite for flatFETs and nanoFETs under illumination.

When the nanoFET is coated with nanoparticles, for example the CTAB-functionalized gold nanorods with the absorption maximum at 800 nm, the negative photoresponse increases. Figure 5.7 shows that by increasing the number of nanorods deposited on the nanoFET an increase in the photoresponse in observed. The analysis of SEM images of the device determines an amount of ~2.5 nanorods/μl. This result outlines the role of the cross-section between the nanorods and the nanowire in controlling the device photoresponse.

This relationship between the photoresponse and the amount of nanoparticles is also accomplished with the other two type of NPs, the spherical ones with λ=520 nm and the nanorods with λ=1400 nm.

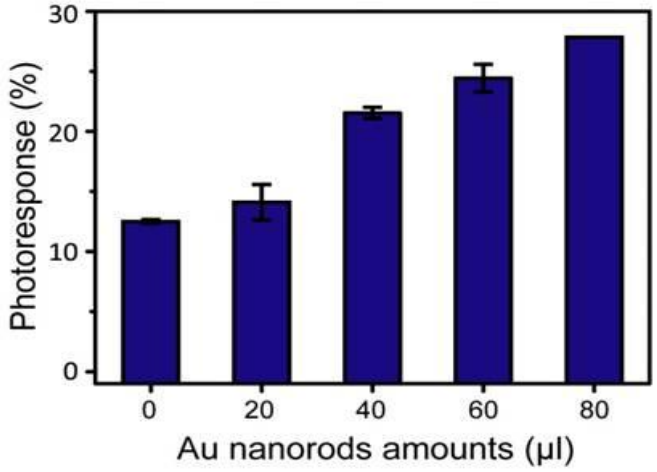

Figure 5.7. Photoresponse as a function of the amount of Au nanorods (λ=800 nm).

The relationship between photoresponse and incident light power is also different between the bare SiNW FET and the device coated with the nanorods. Figure 5.8a shows that there is a weakly non-linear dependence in the case of a bare SiNW FET. However, when the device is coated with the nanorods, the photoresponse dependence on the illumination power exhibits two distinct regimes with a transition intensity of ≈ 50 µW/cm^2, as shown in figure 5.8b.

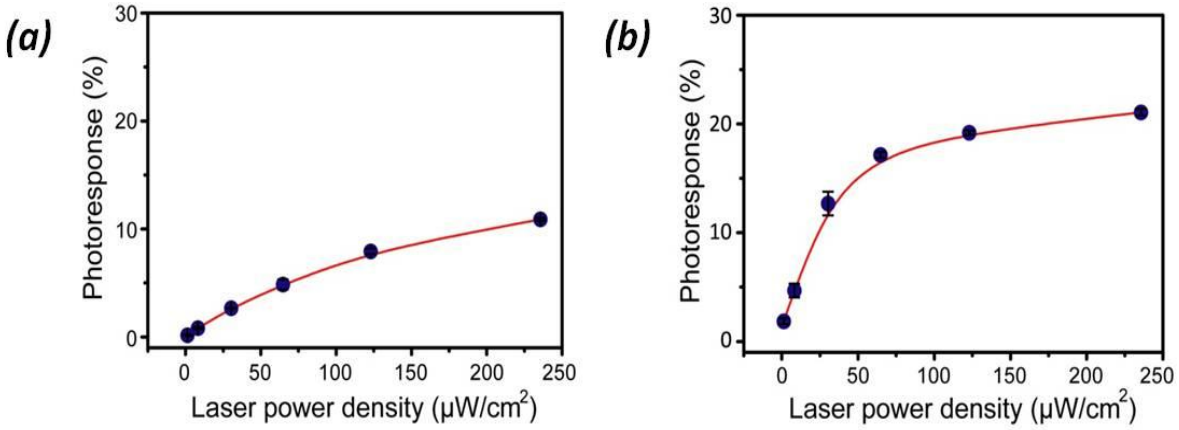

Figure 5.8. (a) Photoresponse as a function of the laser power density for a bare nanoFET. (b) Photoresponse as a function of the laser power density for a nanoFET coated with nanorods. The photoresponse dependence on the illumination power changes when the nanoFET is decorated with Au NPs.

Another change observed when the nanoparticles decorate the nanoFETs is the dependence of the photoresponse on the gate voltage. The measured response in the case of bare nanoFETs is mostly independent of the gate voltage (figure 5.9a), while the device coated with the nanorods shows a significant dependence of the photocurrent on

the gate voltage (figure 5.9b). This is probably related to a capacitive coupling mechanism between the nanowire and the nanorods.

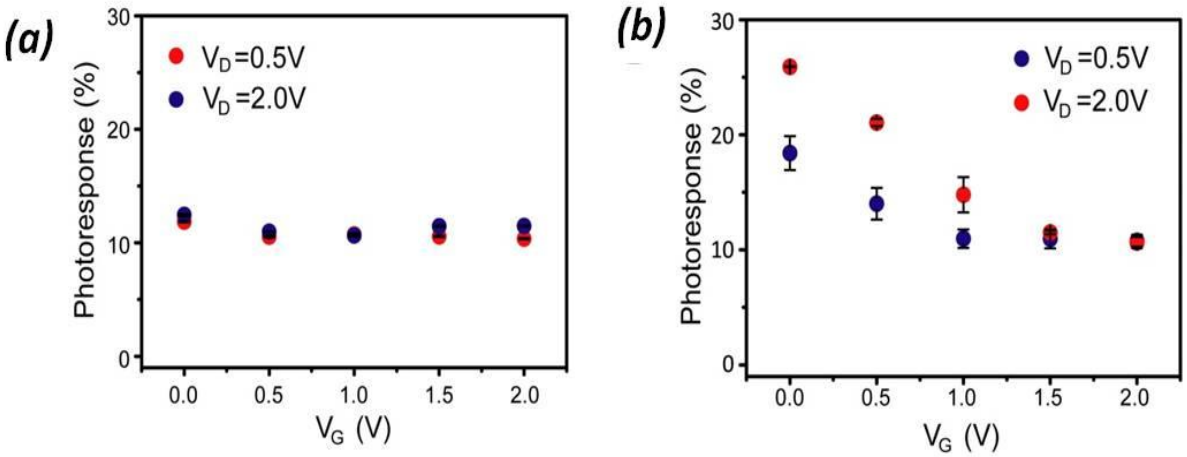

Figure 5.9. Photoresponse as a function of the gate voltage for (a) a bare nanoFET and (b) a nanoFET coated with nanorods.

The decrease in the photoresponse is also observed when the nanoFET is illuminated upon green light. In figure 5.10a it is represented a bare nanoFET with a photoresponse of 2.9%. The negative photoresponse increases to 8.3% when the same device is coated with the spherical Au NPs with λ=520 nm (figure 5.10b).

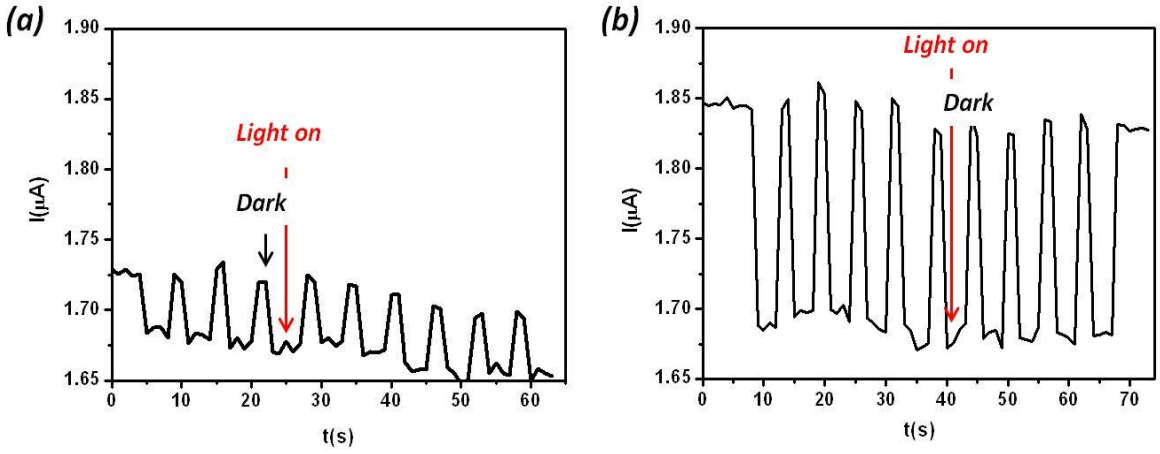

Figure 5.10. I(t) curves showing the device response under dark and green light illumination cycles for (a) a bare nanoFET and (b) the nanoFET coated with the spherical Au NPs (λ=520 nm). Both curves are represented at the same scale.

Finally, the sensitivity of the nanoFET+Au NPs device to different wavelengths is shown in figure 5.11, where the photoresponse is represented as a function of the gate voltage for bare nanoFETs and nanoFETs coated with the three different nanoparticles. The bare SiNW does not present photoresponse when it is illuminated under λ=1550 nm. This situation changes when it is coated with the Au nanorods with an absorption maximum at 1400 nm. This result shows that the plasmon resonances of the nanoparticles enhance the spectral response of the device.

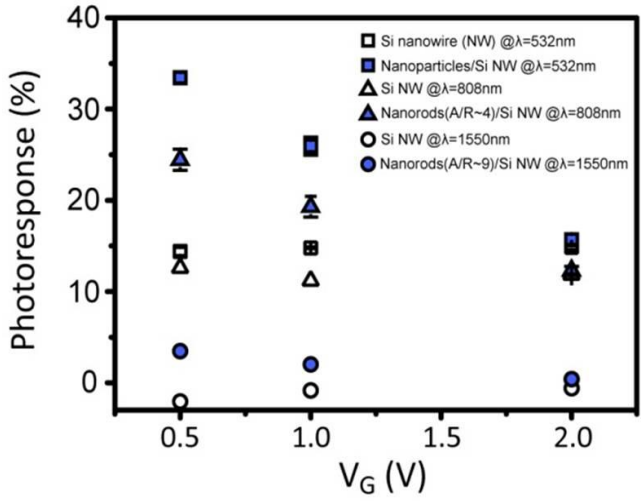

Figure 5.11. Photoresponse as a function of the gate voltage for bare nanoFETs and nanoFETs coated with different CTAB-Au NPs, under their corresponding laser illumination.

The coupling mechanisms between the nanowire surface and the attached Au nanoparticles that lead to the negative photoresponse under illumination is not understood yet, but the sensitivity and the selectivity of the hybrid nanodevice for different wavelengths is demonstrated, making this device interesting as a tunable photodetector.

5. 2. Fabrication of a MoS_2 thin layer field-effect transistor

5.2.1 Introduction

Molybdenum disulfide (MoS_2) is a transition-metal dichalcogenide semiconductor [224]. Currently, there are two main methods to obtain MoS_2 layer flakes: scotch tape cleavage [225] and chemical vapor deposition (CVD) synthesis [226]. MoS_2 monolayer has a thickness of 6.5 Å [224]. This material presents a direct bandgap of 1.8 eV [227] which makes it interesting for optoelectronic applications, such as ultrasensitive photodetectors

[228] and good mechanical properties [229]. The MoS_2 monolayer FETs with HfO_2 as the gate dielectric present on/off ratios exceeding 10^8 at room temperature [230]. The good electrical properties joined with a large active area available in the order of microns with respect to the atomic thickness make the MoS_2 thin layer FETs suitable to free-label biosensors [231-232]. Recently, the use of nanopores on MoS_2 to study the translocation events of various types of DNA has been reported [233]. The ability of o-SPL to make modifications in a wide range of materials is validated for this material.

The patterning of o-SPL structures on MoS_2 thin layer FETs to reduce the size of the transistor is presented in this section. This work is being developed in collaboration with Prof. Andras Kis research group, LANES, at EPFL, Lausanne.

5.2.2 Decreasing of the transistor channel by o-SPL

The starting point is a chip containing the MoS_2 thin layer FETs. The MoS_2 flakes are synthesized by CVD and deposited on a silicon substrate with a 270 nm thick SiO_2 layer. Then, some of the flakes are contacted by EBL with gold. The silicon is used as the back gate, the silicon oxide and the Au contacts act as the dielectric layer and the source/drain electrodes, respectively. A scheme of the device is represented in figure 5.12a.

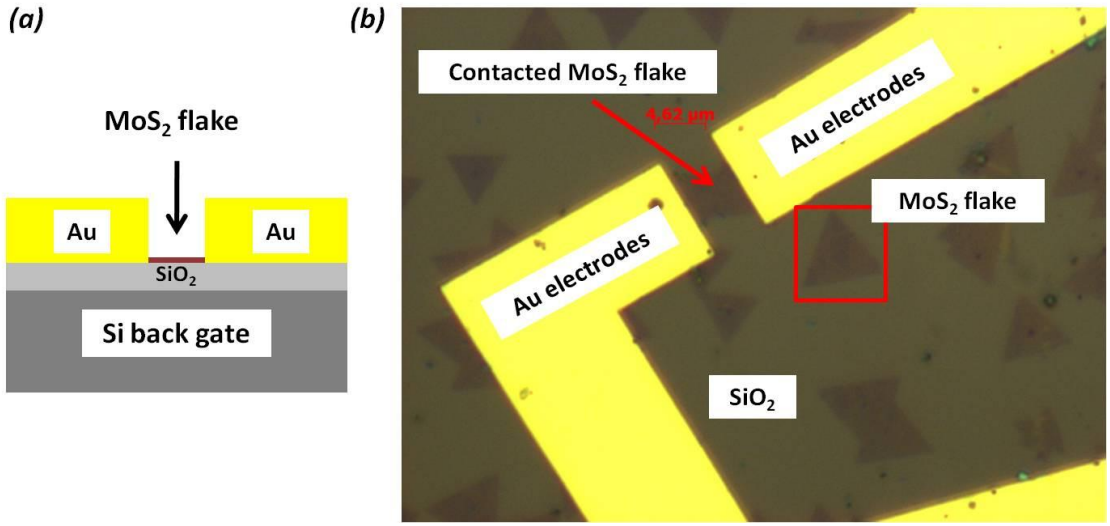

Figure 5.12. (a) Scheme of the device. The MoS_2 thin layer is the transistor channel of the back gated field-effect transistor. (b) Optical image of the device. One of the MoS_2 flakes is contacted with gold electrodes by EBL. The flakes lie on a 270 nm thick SiO_2 layer.

The transistor on which o-SPL was performed is represented by an optical image in figure 5.12b and by an AFM topographic image in figure 5.13. The area of the flake between the electrodes is in the order of μm^2.

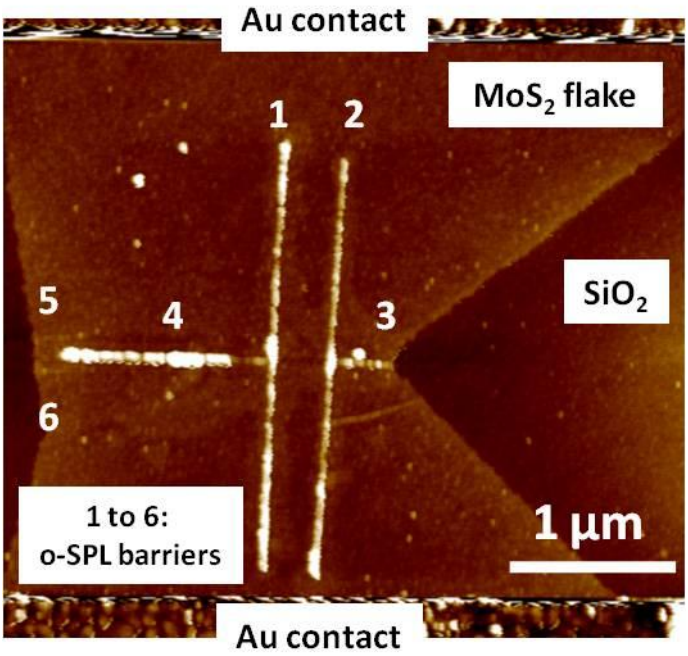

Figure 5.13. AFM image of a MoS_2 thin layer FET after the fabrication of six insulating barriers by oxidation scanning probe lithography.

Six barriers were made by o-SPL to reduce the size of the conduction channel, labeled as 1 to 6 in figure 5.13. The oxidation conditions were 54 V of pulse voltage, 250 µs of oxidation time and 8 nm of free amplitude. UV light was applied during 15 minutes inside the chamber to generate an atmosphere of ozone. The purpose of working with a certain amount of ozone was to restrict the extension of the area of modification produced by the oxidation process under water vapor ambient (figure 5.14).

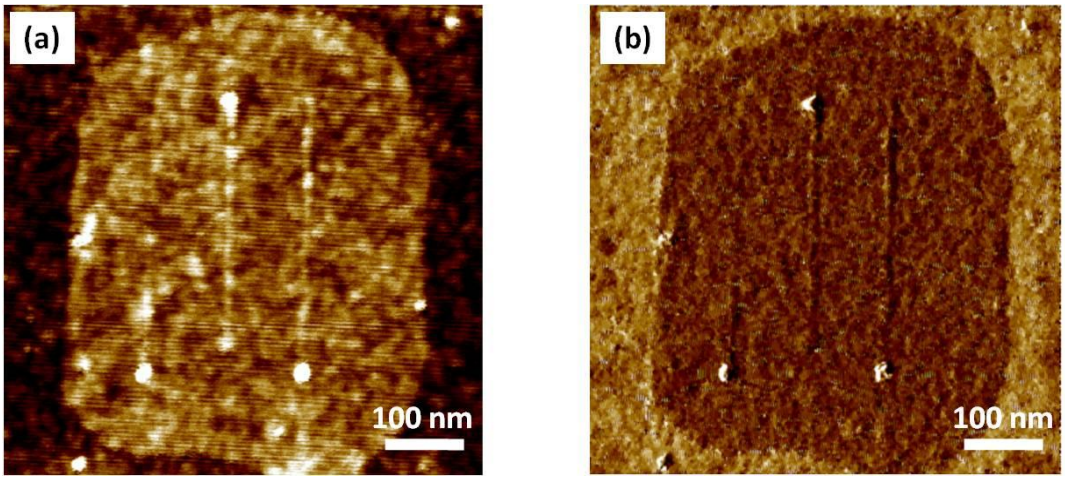

Figure 5.14. AFM (a) topographic and (b) phase image of three lines patterned by o-SPL on MoS_2 thin layer surface by applying 30V, 5 ms, 44% and 6 nm. The oxidation does not limit only to the programmed structures, but extends to a large portion of area which surrounds them.

The o-SPL barriers have widths in the range of 43 to 50 nm and heights in the range of 4.8 to 6.7 nm. The width of the channel has been reduced from a few microns to about 300 nm.

5.2.3 Electrical measurements of the MoS_2 devices.

To check the effect of the decrease in the channel size on the transistor conduction, the output curves of the devices before and after the o-SPL process are compared in figures 5.15a and 5.15b, respectively. From figure 5.15b, it can be seen that after the fabrication of the o-SPL barriers, there is a reduction in the current of two orders of magnitude. The expected result, as the decrease in the size of the channel involves the increase in the resistance of the device. Another observation is that the new transistor saturates for smaller values of source drain voltage. The measurements are performed at room temperature.

The further reduction in size of the MoS_2 channel is planned to fabricate one dimensional (1D) devices such as quantum dots.

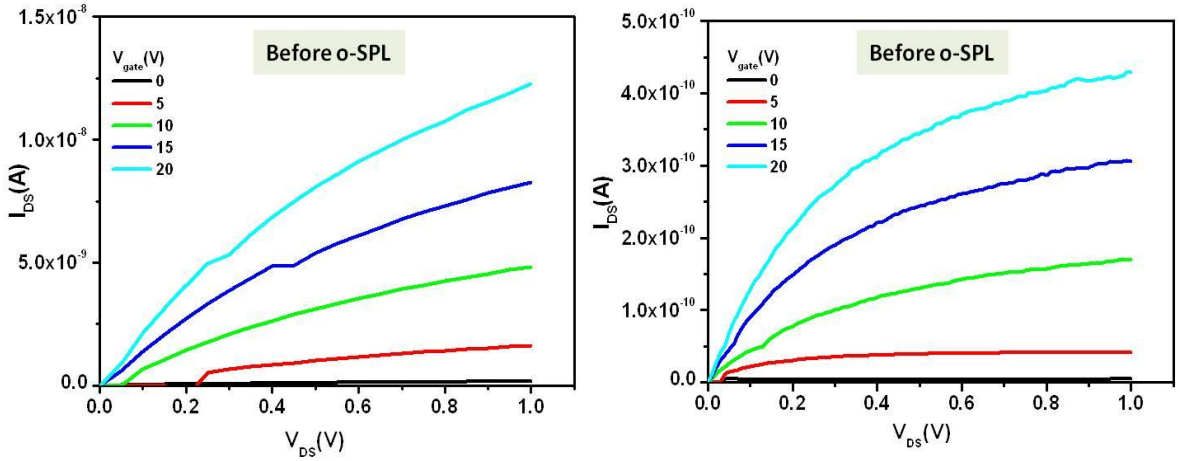

Figure 5.15. Output curves of (a) the MoS_2 thin layer FET as shown in figure 4.2a, (b) the same device after the fabrication of o-SPL barriers, as shown in figure 4.2b.

5.3. Chapter summary

The main points of the chapter are:

- The photoresponse of o-SPL fabricated SiNW FETs decorated with functionalized Au NPs under illumination at different wavelengths (λ=532 nm, 808 nm and 1550 nm) has been studied. The experiments show that the presence of nanoparticles in the surface of the nanowires enhances the photoresponse. Moreover, in the case of λ=1550 nm, only the SiNW+Au NPs configuration gives

photoresponse, while it is zero when the bare SiNW is illuminated. This nanowire-nanoparticles system constitutes an example of hybrid nanodevice.

- An example of the application of o-SPL to fabricate electronic devices different to silicon-based ones is the decreasing of the channel of a MoS_2 thin layer field-effect transistor by the creation of insulating barriers to confine the conduction area.

General conclusions

- An array of 50 lines with a length of 250 nm, a periodicity of 15 nm and an average width of 7.5 nm at FWHM was fabricated, as an example of the sub-10 nm resolution achievable with the technique.

- After rapid thermal annealing treatment, the electron mobility and the subthreshold swing of the silicon nanowire field-effect transistors fabricated by o-SPL are, respectively, about 200 cm^2/Vs and 500 mV/dec. These values are almost identical to the values of similar devices fabricated by EBL in this thesis and comparable with the values of similar devices fabricated by other top-down and bottom-up methods found in the literature.

- The previous point addresses that the electrical properties of the SiNWs are intrinsic and depend only on the geometry, not in the lithographic method.

- The o-SPL fabricated transistors present good device performance. The high subthreshold swing of 500 mV/dec is mainly controlled by the back gate configuration and the thickness of the SOI dielectric layer.

- An ultra thin SOI substrate (12 nm top Si layer, 25 nm BOX) has been employed to fabricate SiNW transistors by o-SPL as a strategy to decrease the size of the channel and to have a thinner dielectric layer. The optimization of the reactive ion etching step allows producing SiNWs which preserve the initial thickness of the Si layer (12 nm) using o-SPL oxide masks 1 nm high.

- Using o-SPL oxide masks with heights smaller than 1 nm, it is possible to fabricate SiNWs with very small cross sections (< 100 nm^2).

- The photoresponse of o-SPL SiNW FETs covered with functionalized Au NPs was studied at different wavelengths. The bare silicon nanowire transistor does not show photoresponse under illumination at 1550 nm, while the transistor decorated with the nanoparticles does present photoresponse for this wavelength. The mechanism is not still understood, but this hybrid nanowire-nanoparticles photodetector is an example of application for the transistors fabricated by o-SPL.

- Another example of application for oxidation scanning probe lithography is the decreasing in the width of a MoS_2 thin layer field-effect transistor from microns to hundreds of nanometers by the creation of insulating barriers to reduce the conduction area.

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